RS9113 n-Link™ Module Family

Datasheet

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Overview

The RS9113 n-Link module family is based on Redpine Signals' RS9113 ultra-low-power, single spatial stream, dual-band 802.11n, BT EDR2.1, BT Low Energy 4.0, ZigBee Convergence SoC. The module is a high performance 2.4GHz/5GHz dual-band module in a cost effective footprint supporting IEEE 802.11n WLAN, BT EDR2.1, BT Low Energy 4.0 and ZigBee 802.15.4 standards. The module integrates a multi-threaded MAC processor called TA processor with integrated analog peripherals and support for digital peripherals, baseband digital signal processor, analog front-end, crystal oscillator, calibration OTP memory, dual-band RF transceiver, dual-band high-power amplifiers, baluns, diplexers, diversity switch and Quad-SPI flash.

The RS9113 n-Link module realizes host-based architecture where necessary MAC and PHY layers are implemented in the device to support WLAN, Bluetooth and ZigBee applications in conjunction with a host processor over SDIO or USB interfaces. The RS9113 n-Link modules are available in two hardware footprints. One footprint type comes with an integrated antenna along u.FL connector and the other module footprint comes without an integrated antenna.

Applications:

- Smartphones, Tablets and e-Readers
- VoWi-Fi phones
- Smart Meters and in-home displays
- Industrial automation and telemetry
- MP3 music and MP4 video players
- Medical Devices
- Industrial monitoring and control
- Home and building automation

Module Features:

- RS9113 n-Link module integrates WLAN, BT and ZigBee functions.
- WLAN: Compliant to IEEE 802.11 a/b/g/n with dual band support.
- Bluetooth: Compliant to BT EDR2.1 and BT Low Energy 4.0
- ZigBee: Compliant to IEEE 802.15.4
- Supports both 20 MHz and 40 MHz channel bandwidth.
- WLAN transmit power up to +18 dBm.
- WLAN receive sensitivity of - 97 dBm.
- Bluetooth transmit power of +18dBm (class-1).
- Bluetooth receiver with -91 dBm Rx sensitivity.
- Support for multiple ZigBee output powers up to +19 dBm with integrated PA.
- High performance ZigBee receiver with -103 dBm Rx sensitivity.
- U.FL connector for external antenna connection is selectable.
- Dual external antenna (diversity supported).
- Seamless integration with 32 bit processors.
- SDIO/USB host interface for WLAN, BT, ZigBee.
- Host driver for Linux, Android and Win CE.
- Single supply 3.0 to 3.6 V operation.

About this Document

This document describes about the RS9113 n-Link module family specifications. The module is based on Redpine Signals' RS9113 ultra-low-power, single spatial stream, dual-band 802.11n +BT EDR2.1 and BT Low Energy 4.0 +ZigBee convergence SoC. The description covers host interface, Wi-Fi, BT and ZigBee features, I/O interface, pin description of the module and electrical characteristics.

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1 Overview

The RS9113 n-Link module is an M2M Combo module which is based on Redpine Signals RS9113 ultra-low-power, single spatial stream, dual-band 802.11n + BT4.0 +ZigBee Convergence SoC. The RS9113 module provides low-cost CMOS integration of a multi-threaded MAC processor, baseband digital signal processing, analog front-end, crystal oscillator, calibration OTP, dual-band RF transceiver, dual-band high-power amplifiers, baluns, diplexers, diversity switch and Quad-SPI Flash thus providing a fully-integrated solution for a range of embedded wireless applications. The RS9113 based chips and modules leverage and improve upon Redpine's proven low power innovations from Lite-Fi™ products (RS9110) and provide WLAN 802.11n, BT4.0 and ZigBee convergence solution for integration into mobile and M2M communication devices. With an advanced CMOS ultra-low-power PMU, integrated analog peripherals and support for a variety of digital peripherals, RS9113 enables very low-cost implementations for wireless embedded and M2M applications. It can connect to a host processor through SDIO, USB, SPI or UART interfaces.

1.1 Block diagram

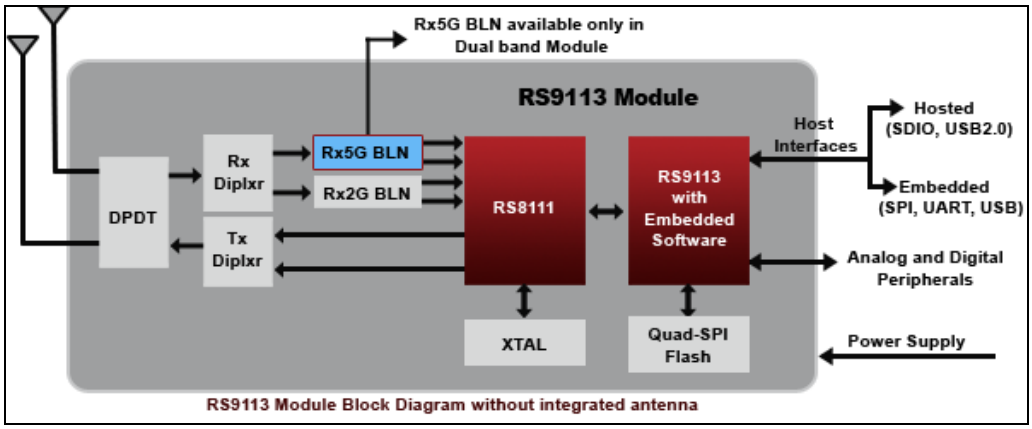


Figure 1: RS9113 Module without Integrated Antenna

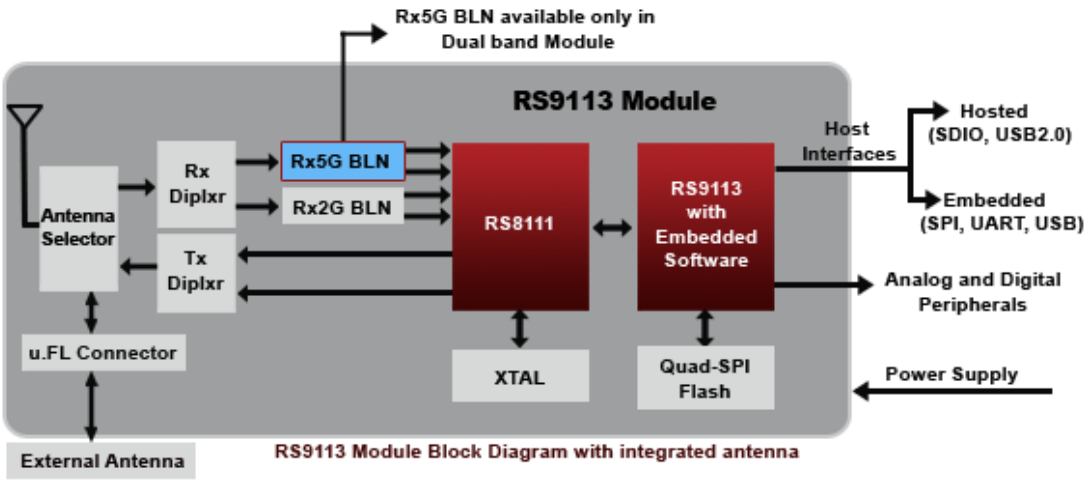


Figure 2: RS9113 Module with Integrated Antenna

1.2 Product Variants

RS9113 n-Link module family has product variants as listed in the following table.

Module Part #	Wi-Fi 2.4GHz	Wi-Fi 5GHz	BT[1]	ZB[2]	Integrated Antenna &u.Fl	SDIO	USB	Package #
RS9113-N00-S0N	Y	N	N	N	N	Y	Y	P6
RS9113-N00-D0N	Y	Y	N	N	N	Y	Y	P6
RS9113-N00-S1N	Y	N	N	N	Y	Y	Y	P7
RS9113-N00-D1N	Y	Y	N	N	Y	Y	Y	P7
RS9113-NB0-S0N	Y	N	Y	N	N	Y	Y	P6
RS9113-NB0-D0N	Y	Y	Y	N	N	Y	Y	P6
RS9113-NB0-S1N	Y	N	Y	N	Y	Y	Y	P7
RS9113-NB0-D1N	Y	Y	Y	N	Y	Y	Y	P7
RS9113-N0Z-S0N	Y	N	N	Y	N	Y	Y	P6
RS9113-N0Z-D0N	Y	Y	N	Y	N	Y	Y	P6
RS9113-N0Z-S1N	Y	N	N	Y	Y	Y	Y	P7
RS9113-N0Z-D1N	Y	Y	N	Y	Y	Y	Y	P7
RS9113-NBZ-S0N	Y	N	Y	Y	N	Y	Y	P6
RS9113-NBZ-D0N	Y	Y	Y	Y	N	Y	Y	P6
RS9113-NBZ-S1N	Y	N	Y	Y	Y	Y	Y	P7
RS9113-NBZ-D1N	Y	Y	Y	Y	Y	Y	Y	P7

[1] BT – BT EDR2.1 / BT Low Energy 4.0
[2] ZB – ZigBee (802.15.4-2009)

Table 1: Product Variants

The following table lists the module package variants.

Module package variant	Package #
Module without integrated antenna	P6
Module with integrated antenna	P7

Table 2: Module Package Variants

2 Features

2.1 Device Features

- Zero load architecture for datapath.
- Ultra-low-power, low-cost and high-throughput 1 Tx – 1 Rx Dual-band 802.11n + BT EDR 2.1 and BT Low Energy 4.0 + ZigBee (802.15.4-2009).
- Data rates up to 150 Mbps using 1-Spatial Stream 802.11n MCS-7, 40MHz bandwidth mode for high user throughput.
- Supports 20MHz and 40MHz bandwidth.
- WLAN transmit output power upto +18 dBm.
- WLAN receiver with -97 dBm Rx sensitivity.
- Bluetooth transmit power output of 20 dBm (class-1).
- Bluetooth receiver with -94 dBm Rx sensitivity.
- High performance ZigBee receiver with -103 dBm Rx sensitivity.
- Support for multiple ZigBee output powers up to +19 dBm.
- Innovative coexistence algorithms for optimum throughput of Wi-Fi and Bluetooth or Wi-Fi and ZigBee operating together.
- Integrated ultra-low-power subsystem with <25uA in RAM retention mode and <6.5uA with no RAM retention.
- Hardware assisted radar detection with compliance to FCC and ETSI norms.
- Advanced power management techniques for power save modes.
- Integrated OTP, crystal oscillator, high power amplifiers, baluns, diplexers, diversity switch and high-speed Quad-SPI Flash resulting in zero external BOM other than antennae.
- Support for multiple host interfaces to allow maximum flexibility for system integration. Host interfaces supported are SDIO and USB 2.0.
- [3]Supports multiple peripheral interfaces GPIO, I2S, PCM, UART and SPI
- Complete software along with host driver for Linux and Android operating systems.
- Operating temperature range is between -40°C and +85°C.
- Single supply 3.0 to 3.6 V operation for the module, As per USB standards we support USB with VBUS voltage as 5.0V.

2.2 Host Interfaces

- SDIO
  - Operation up to a maximum clock speed of 50 MHz
  - SDIO standard version 2.0 compatible.
  - Supports4-bit SDIO modes.

[3] Peripheral interfaces are not available by default, please contact Redpine for Specific peripheral.

- USB 2.0
  - Supports 480Mbps "High Speed" (HS), 12Mbps "Full Speed" (FS).

2.3 WLAN Features

2.3.1 MAC

- Conforms to IEEE 802.11a/b/g/n standards for MAC
- Hardware accelerators for WEP 64/128-bit, TKIP, AES and WAPI.
- Hardware accelerators for WPS.
- Hardware support for IPsec offload and TCP checksum offload.
- Support for security protocols WPA, WPA2.
- Support for WMM.
- AMPDU and AMSDU aggregation/de-aggregation for high performance
- Dynamic selection of fragment threshold, data rate, and antenna depending on the channel statistics

2.3.2 Baseband Processing

- Supports DSSS (1, 2 Mbps) and CCK (5.5, 11 Mbps) modes
- Supports all OFDM data rates (6, 9, 12, 18, 24, 36, 48, and 54 Mbps, MCS0 to MCS7, MCS32)
- Supports IEEE 802.11n single-stream modes with data rates up to 150 Mbps
- Supports long, short, and HT preamble modes
- High-performance multipath compensation in OFDM, DSSS, and CCK modes

2.4 Bluetooth Features

- Supports BT EDR 2.1 and BT Low Energy 4.0
- USB and SDIO Host interfaces
- Bt master mode can support upto 7 slaves.
- Bluetooth security features: Authentication, Pairing and Encryption
- Supports low power connection states such as hold, sniff and park modes with selectable sniff intervals.
- Proprietary FEC for DQPSK and 8-PSK modes.
- Provides finer granularity of range vs. throughput control.
- Wireless coexistence.

2.5 ZigBee Features

2.5.1 MAC

- Zigbee Stack: Zigbee pro stack residing inside the module.

- Supporting mode: ZigBee Coordinator, Router, End device
- PHY features: Beacon, Non-Beacon, CCM Security, Promiscuous mode
- Power saving using End Device Sleep, network periodic sleep
- Supports CCM* Security levels 1-7
- Supports Active scan, channel selection, Association and Disassociation, Orphan scanning, and coordinator realignment

2.5.2 Profiles

- Profiles are part of application and the module supports any profile with its transparent mode of data transmission and reception.

2.5.3 Baseband processing

- Supports IEEE 802.15.4-2009, 250kbps

2.6 Co – Existence arbiter

- Arbitration between Wi-Fi, BT and Wi-Fi, ZigBee.
- Application aware arbitration.
- QoS assurance across different wireless traffic.

2.7 Peripherals

- One UART interface with programmable baud-rate generator.
- GPIO and LED interfaces.
- SPI interface.
- PCM interface.
- I2S interface.
- Debug UART interface.

2.8 RF transceiver

- Highly integrated 2.4 GHz transceiver with direct conversion architecture.
- Receiver with 38 dB RF selectable gain range and 60 dB baseband variable gain range.
- Power amplifier with 19 dBm maximum output power.
- Integrated LNA, BPF, and T/R switch.

2.9 Software

- OneBox-Mobile™ software supports 802.11abgn Access Point, Client and Wi-Fi Direct, dual-mode BT 4.0, ZigBee(802.15.4-2009)

and SEP 2.0 functionality on a variety of host platforms and operating systems.

- The software package includes complete firmware, reference drivers, application profiles and configuration interface for , Linux and Android operating systems.
- Wi-Fi driver supports Client mode or Access point mode or Wi-Fi Direct mode.
- Wi-Fi driver has support for simultaneous Client mode and Access point/Wi-Fi Direct Group Owner (GO) mode.
- Bluetooth host driver utilizes open source host stacks like BlueZ for Linux and Bluedroid for Android, which support the following layers
  - L2CAP
  - RFCOMM
  - BNEP
  - CMTP
  - HIDP
  - HCI
  - SMP
- Application layer supports all profiles supported by BlueZ on Linux and Bluedroid on Android.
- Profiles are part of application and the module supports any profile with its transparent mode of data transmission and reception.

2.10 Power save

In order to save battery power, the MAC can perform clock gating of the unused blocks or transit the system from Normal mode to Low Power (LP) or ultra Low Power (ULP) modes. LP modes are supported by USB and SDIO supports both LP and ULP modes.

In LP mode, the modem is shutdown and the SoC is not powered down. Sleep state machine in the SoC is active and responds to wake-up events. Host interface is active and TA processor can take packets from host even during sleep.

In ULP mode, the entire chip except the ULP sub-system will be shut down. Host interface is not active in this mode. Entry into sleep state is notified by the device to host. The host shall hold subsequent packets to be sent to the device until it gets notified about device's exit from sleep state.

The module can be programmed to go into standby mode (deep-sleep) and standby-associated mode.

2.10.1 Features

- Operates on very low power consuming 32 KHz internal clock.
- Provides six modes of wake-up.

- Waits for oscillator to settle down before un-gating the clock to SoC.

2.10.2 Operation

After turning off all the modules software will determine the amount of time to be slept and configure the same in sleep state machine's registers and issues sleep start command.

During the sleep time, host clock is fed to the processor when some host command is received. Processor has to serve these requests during this time with minimum latency. The clock will be gated immediately after the completion of the command at the host interface.

2.10.3 Wake-up modes

The following are the various wake-up modes supported

- Sleep timeout.
- Host request.
- Request from TA processor.
- GPIO pin based wake-up.
- ULP timer wake-up.
- Sleep clock timer timeout.

3 Package Description

3.1 Package description for module without integrated antenna (Package # P6)

3.1.1 Mechanical Characteristics

Parameter	Value(L x W x H)	Tolerance	Unit
Module imension for P6	14 x 15 x 2.1	±0.1	mm

Table 3: Mechanical Characteristics

3.1.2 Package Dimensions

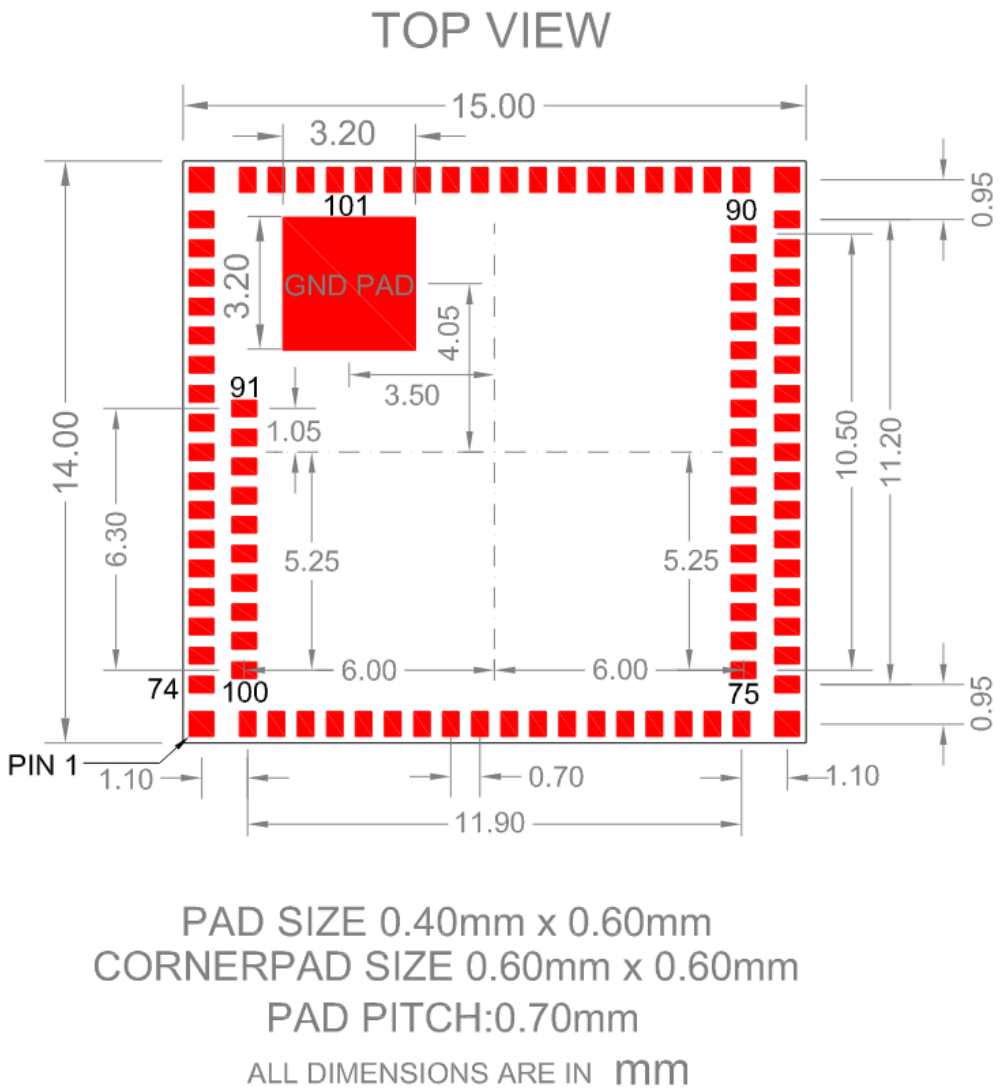


Figure 3: Module Package and Pad Dimensions

3.1.3 PCB Landing Pattern Dimensions

These dimensions are the foot print of the module to be used for PCB layout.

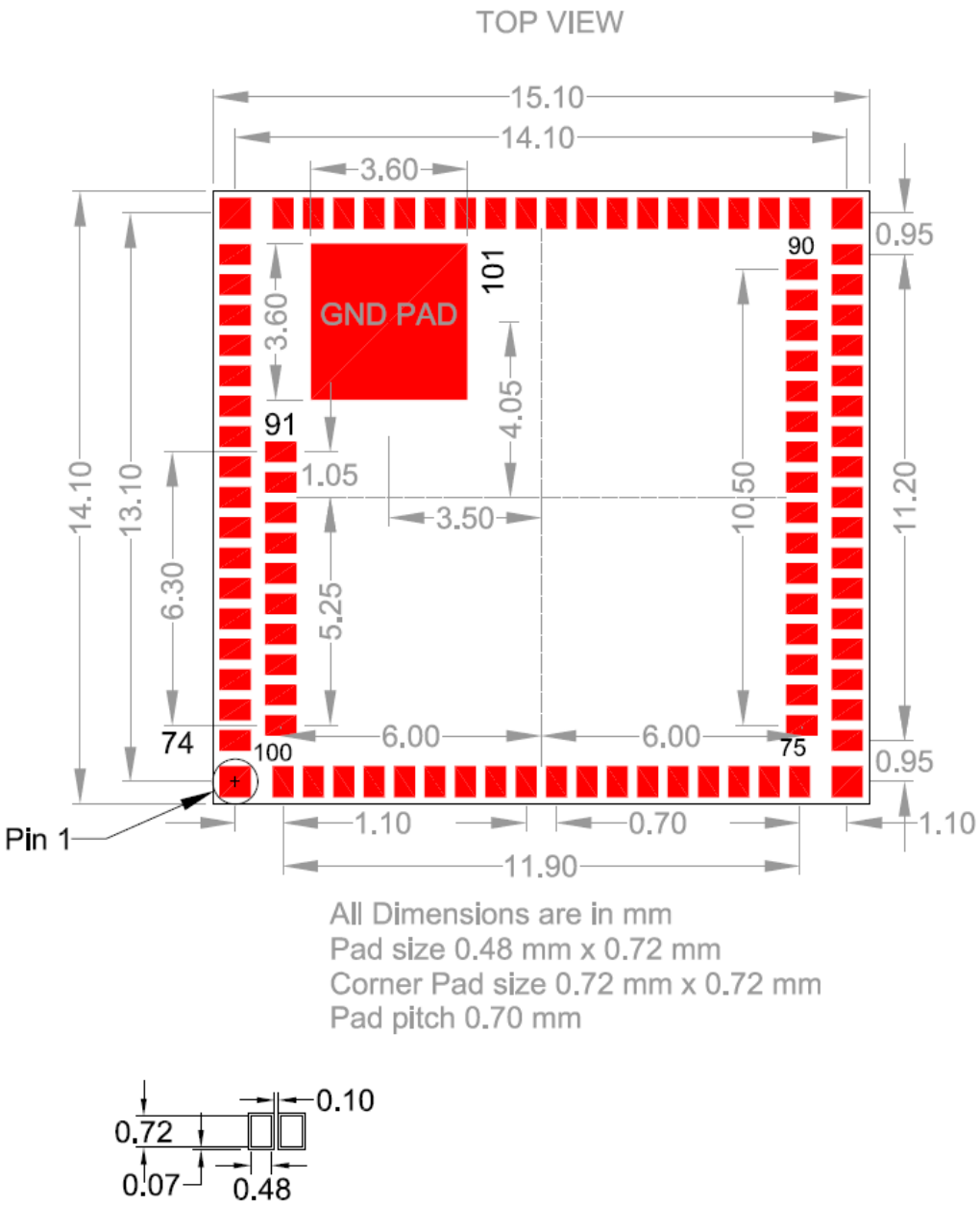


Figure 4: PCB Landing Pattern Dimensions

3.2 Package description for module with integrated antenna (Package # P7)

3.2.1 Mechanical characteristics

Parameter	Value(L x W x H)	Tolerance	Unit

Module dimension	27 x 16 x 3.1	±0.1	mm

Table 4: Mechanical Characteristics

3.2.2 Package Dimensions

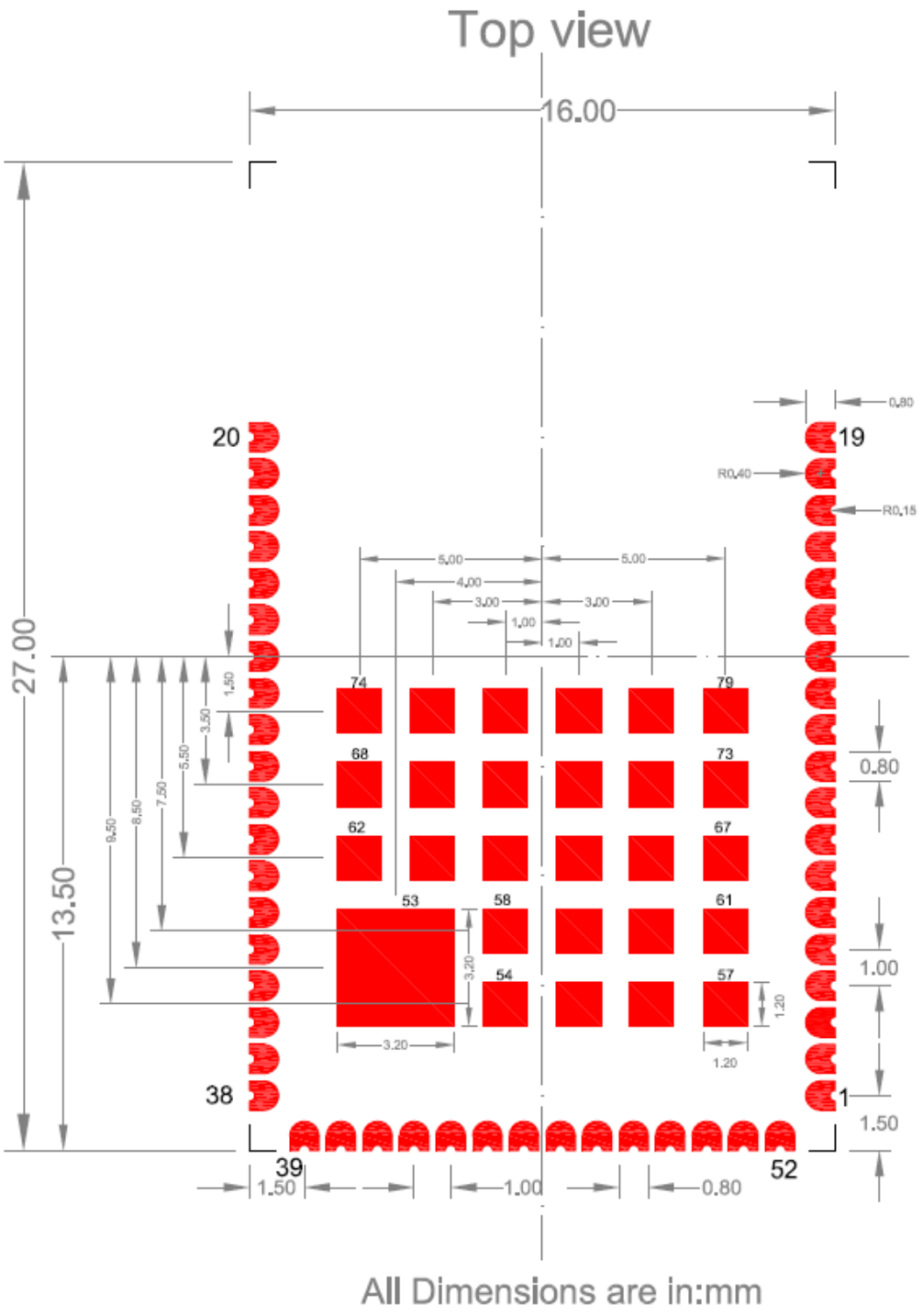


Figure 5: Module package and pad dimensions

3.2.3 PCB Landing Pattern Dimensions

These dimensions are the foot print of the module to be used for PCB layout.

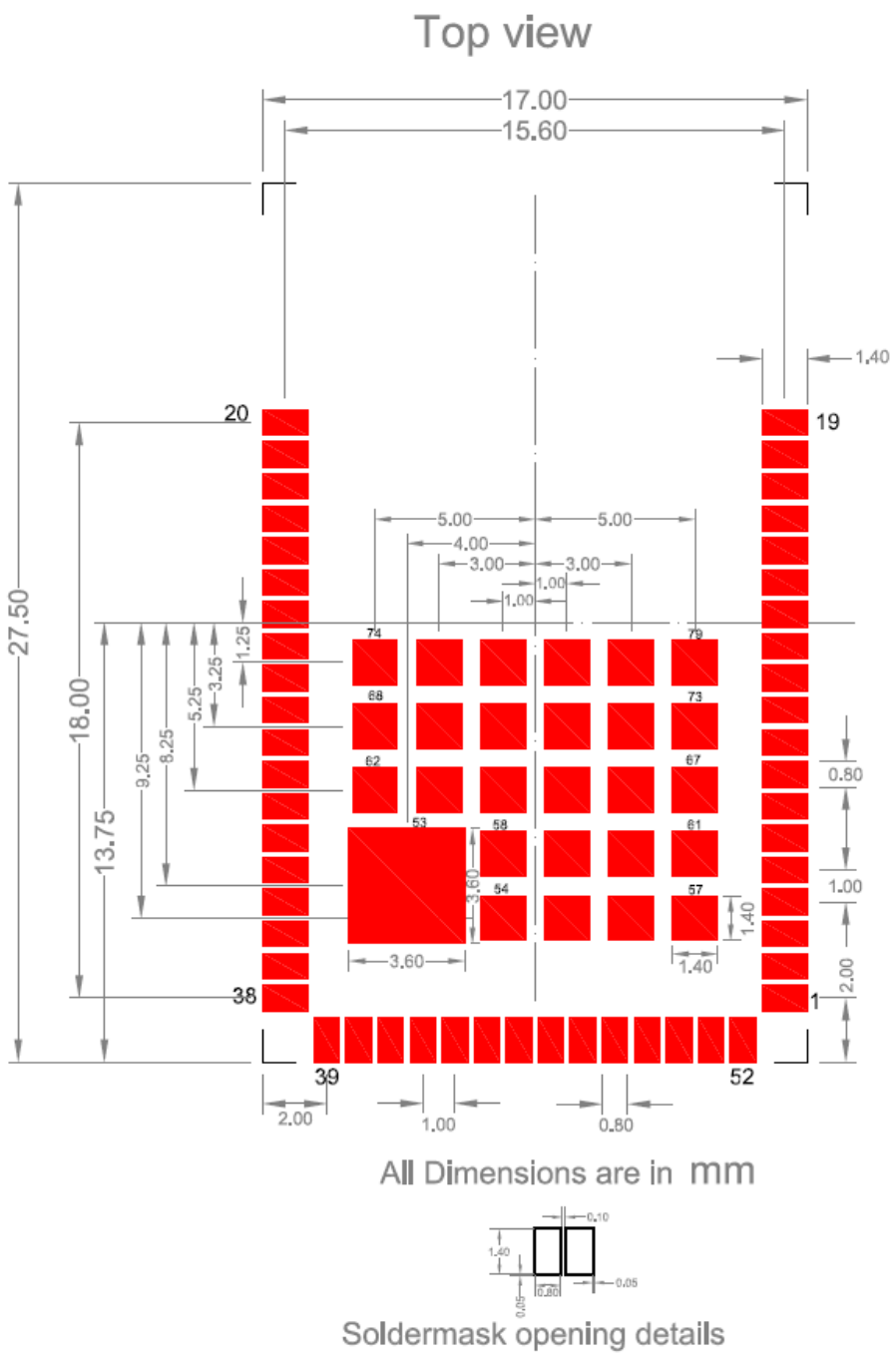


Figure 6: PCB landing pattern dimensions

3.3 Recommended Reflow Profile

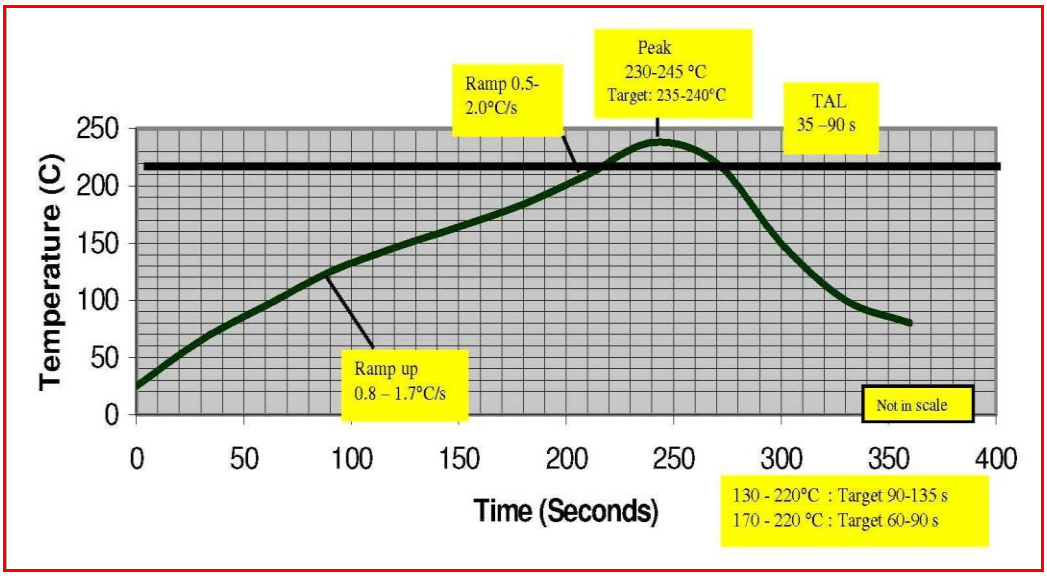


Figure 7: Reflow Profile

NOTE: The profile shown is based on SAC 305 solder (96.5% Tin, 3% silver, 0.5% copper). We recommend the ALPHA OM-338 lead-free solder paste. This profile is provided mainly for guidance. The total dwell time depends on the thermal mass of the assembled board and the sensitivity of the components on it. The recommended belt speed is 50-60 Cm/Min. A finished module can go through 2 more reflow processes.

3.4 Baking Instructions

The RS9113 module package is compliant to MSL-3. It is a moisture sensitive device and must be handled appropriately. After the devices are removed from their vacuum sealed packs, they should be taken through reflow for board assembly within 168 hours during which time; they are expected to be stored at MSL-3 environmental conditions (less than 60% relative humidity and 30° C). If these conditions are not met, the devices must be baked before reflow. The recommended baking time is nine hours at 125°C

4 Pin Description

4.1 Pin description for module without integrated antenna

4.1.1 Module Pinout Diagram

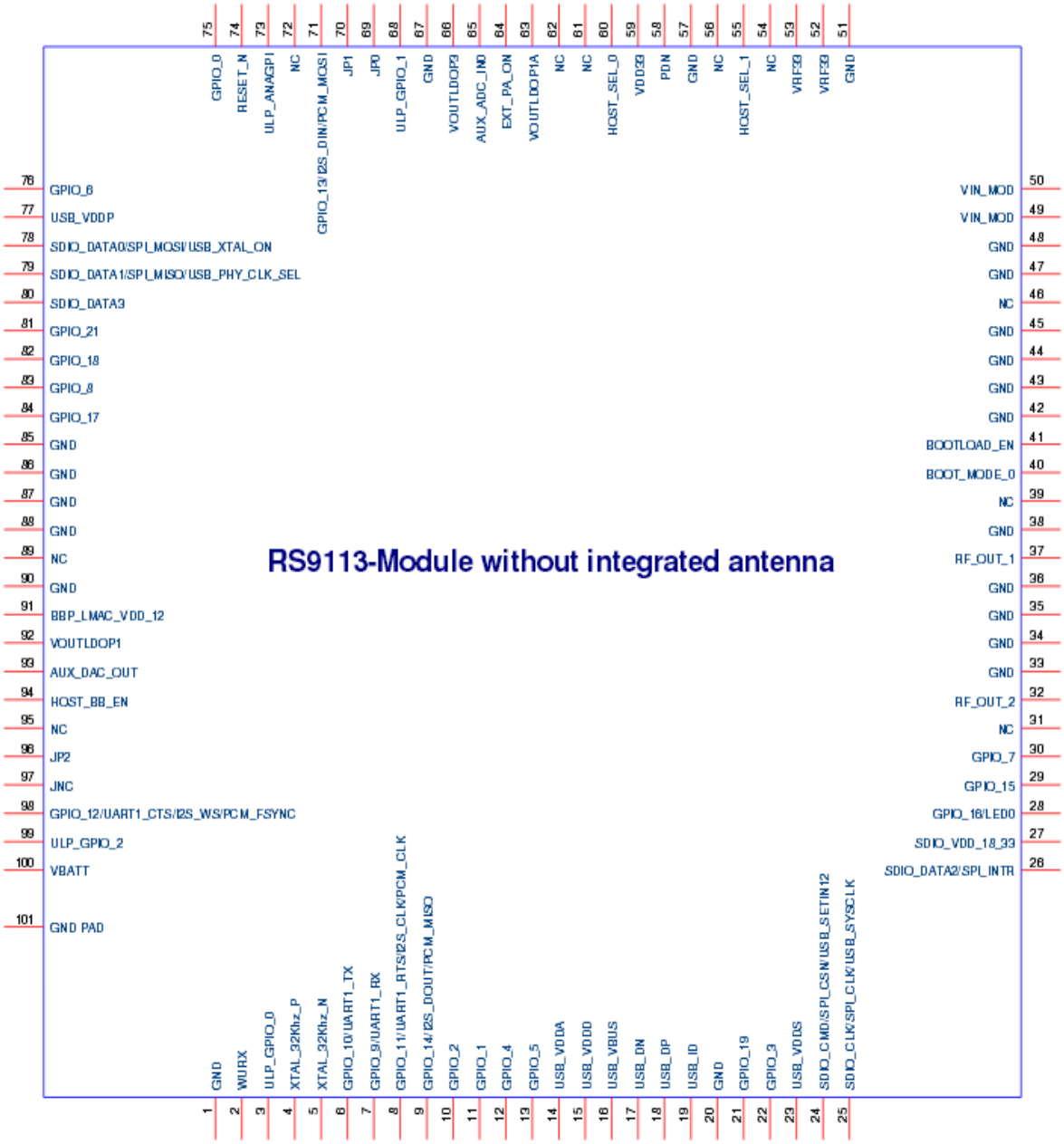


Figure 8: Module Pinout Diagram

4.1.2 Pin Description

This section describes the pins of RS9113 module without integrated antenna

4.1.2.1 Control and RF Interface

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	XTAL_32Khz_N	5	Input	32kHz off-chip crystal connection for accurate wake-up time. Not supported in the current firmware.should be left open.
2.	XTAL_32Khz_P	4	Input	
3.	EXT_PA_ON	64	Output	Signal to enable external power amplifier. Not Supported in the current firmware should be left open.
4.	RF_OUT_2	32	RF In/RF Out	Default Antenna port (50 ohms impedance). If unused, this pin should be left open.
5.	RF_OUT_1	37	RF In/RF Out	Antenna port (50 ohms impedance). If unused, this pin should be left open.
6.	WURX	2	Input	This pin is used for wireless RF wake-up. If RF wake-up feature is used, then route the PCB trace from the output of this pin, as a 50 ohms RF line. Not supported in the currentfirmware.should be left open..
7.	RESET_N	74	Input	Active-low asynchronous reset signal. The reset assertion time is about 20 ms.
8.	PDN	58	Input	Reserved (connect this pin to ground through a 100k ohms pull-down resistor).

S.No.	Pin Name	Pin number	Direction	Pin Description
9.	NC	31,39, 46, 54,56,61,62, 72,89,95	NC(Not Connected)	These pins should be left as No connects.

Table 5: Control and RF Interface

4.1.2.2 Power and Ground Interface

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	SDIO_VDD_18_33	27	Input	SDIO mode: 1.8V or 3.3V digital power supply. Based on SDIO data lines operating volatge.
			Input	Other modes: 3.3 V digital power supply.
2.	BBP_LMAC_VDD_12	91	Input	Digital power supply for RS9113 module. This pin should be connected to VOUTLDOP1A (pin # 63).
3.	USB_VDDA	14	Input	USB mode: 3.3V analog power supply.
			Input	Other modes: Connect this pin to ground.
4.	USB_VDDS	23	Input	USB mode: 3.3V digital power supply.
			Input	Other modes: Connect this pin to ground.
5.	USB_VDDP	77	Input	USB mode: 1.2V analog power supply. This pin should be connected to VOUTLDOP3 (pin # 66). No external supply needed
			Input	Other modes: Connect this pin to ground.
6.	USB_VDDD	15	Input	USB mode: 1.2V digital power supply. This pin should be connected to VOUTLDOP1 (pin # 92). No external supply

S.No.	Pin Name	Pin number	Direction	Pin Description
				needed.
			Input	Other modes: Connect this pin to ground.
7.	VIN_MOD	49,50	Input	3.3V digital power supply for power management section of RS9113 module.
8.	VRF33	52,53	Input	3.3V analog power supply for RF transceiver. Refer MIG for power supply filter.
9.	VDD33	59	Input	3.3V digital power supply for RF transceiver.
10.	GND	1,20,33,34,35,36,38,42,43,44,45,47,48,51,57,67,85,86,87,88,90	Ground	Common Ground
11.	GND PAD	101	Ground	Central ground pad.

Table 6: Power and Ground Interface

4.1.2.3 SDIO and USB Interface

The following table lists the pins used to connect to an MCU, with the RS9113 being a slave, using SDIO or USB. The pins are configured for a particular interface by controlling the HOST_SEL[1:0] reset latches- please refer to section 4.1.2.9 for further details on reset latch configuration. All SDIO signals of type LVCMOS are rated at 8mA. All USB signals except USB_VBUS are analog signals. USB_VBUS is a 5V pin.

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	SDIO_CLK/SPI_CLK/USB_SYSCLK	25	Input	SDIO Mode: This signal is SDIO clock.
			Input	SPI Mode: This signal is SPI clock.

S.No.	Pin Name	Pin number	Direction	Pin Description
			Input	USB Mode: Reserved.
2.	SDIO_CMD/SPI_CSN/USB_SETIN12	24	Input/Output	SDIO Mode: SDIO interface command signal. In UART only host select configuration, connect this pin to ground through a 50k ohms pull-down resistor.
			Input	SPI Mode: Active-low SPI Chip Select signal.
			Input	USB Mode: Reserved.
3.	SDIO_DATA0/SPI_MOSI/USB_XTAL_ON	78	Input/Output	SDIO Mode: Data0 of SDIO interface.
			Input	SPI Mode: SPI Master-Out-Slave-In.
			Output	USB Mode: Reserved.
4.	SDIO_DATA1/SPI_MISO/USB_PHY_CLK_SEL	79	Input/Output	SDIO Mode: Data1 of SDIO interface.
			Output	SPI Mode: SPI Master-In-Slave-Out.
			Input	USB Mode: Connect this pin to ground through a 4.7k ohms pull-down resistor.
5.	SDIO_DATA2/SPI_INTR	26	Input/Output	SDIO Mode: Data2 of SDIO interface.

S.No.	Pin Name	Pin number	Direction	Pin Description
			Output	SPI Mode: Interrupt signal to Host MCU. Active-high level, Active-low level and open-drain modes are supported. Refer MIG for further details.
			Input/Output	USB Mode: Leave this pin as NC.
6.	SDIO_DATA3	80	Input/Output	SDIO Mode: Data3 of SDIO interface. USB Mode: Reserved.
			Output	SPI mode: Active-high level interrupt to Host indicating an error on the SPI bus. When this signal goes high, it indicates that the internal processor has reset the SPI interface due to an error reported by the interface. The Host MCU has to suspend all SPI transactions and re-initialize the SPI once this signal goes low.
			Input/Output	USB Mode: Leave this pin as NC.
7.	USB_VBUS	16	Input	USB mode: 5V power supply.
			Input/Output	Other modes: Leave this pin as NC.
8.	USB_DN	17	Input/Output	USB mode: Negative output channel that is connected to the serial USB cable.
			Input/Output	Other modes: Leave this pin as NC.
9.	USB_DP	18	Input/Output	USB mode: Positive output channel that is connected to the serial USB cable.
			Input/Output	Other modes: Leave this pin as NC.

S.No.	Pin Name	Pin number	Direction	Pin Description
10.	USB_ID	19	Input/Output	USB mode: Connect the USB ID pin to mini-AB receptacle connector.
			Input/Output	Other modes: Leave this pin as NC.

Table 7: SDIO, Slave-SPI and USB Interface

4.1.2.4 GPIO Interface

The RS9113 module has General Purpose I/Os, each with multiple alternate functionalities. All the GPIO pins are reserved by default with exception for few pins described below in the table. Custom firmware modifications are required to enable them to be used as GPIO input/output pins with exception for UART (TX, RX, RTS and CTS). On power up all the GPIO's are Input until the firmware inside the module takes over the default input state.

All GPIO signals of type LVCMOS are rated at 4mA.

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	GPIO_0	75	Input/Output	Reserved Connect this pin to ground through a pull-down resistor of 100k ohms.
2.	GPIO_1	11	Input/Output	Reserved, Connect this pin to a pull-up resistor of 100k ohms.
3.	GPIO_2	10	Input/Output	This pin is configured as Output pin in power save modes. If not used leave this pin as NC.
4.	GPIO_3	22	Input/Output	Reserved. Connect this pin to a pull-up resistor of 100k ohms.
5.	GPIO_4	12	Input/Output	Reserved. Connect this pin to a pull-up resistor of 100k ohms.
6.	GPIO_5	13	Input/Output	Reserved. Connect this pin to a pull-up resistor of 100k ohms.

S.No.	Pin Name	Pin number	Direction	Pin Description
7.	GPIO_6	76	Input/Output	Reserved. Connect this pin to a pull-up resistor of 100k ohms.
8.	GPIO_7	30	Input/Output	Reserved leave this pin as NC.
9.	GPIO_8	83	Input/Output	Reserved leave this pin as NC.
10	GPIO_9/UART1_RX	7	Input/Output	General Purpose Digital Input/Output Pin
			Input	UART1_RX – UART 1 Serial Input. This pin is configured as UART pin based on host selection configuration.
11	GPIO_10/UART1_TX	6	Input/Output	General Purpose Digital Input/Output Pin
			Output	UART1_TX – UART 1 Serial Output. This pin is configured as UART pin based on host selection configuration.
12	GPIO_11/UART1_RTS/I2S_CLK/PCM_CLK	8	Input/Output	General Purpose Digital Input/Output Pin
			Output	UART1_RTS – UART 1 Request To Send. This pin is configured as UART pin based on host selection configuration. When this pin is used, I2S_CLK/PCM_CLK is not functional.
			Input	I2S_CLK – I2S Clock. When this pin is used UART1_RTS is not functional. Not available with the current firmware.
			Input	PCM_CLK – PCM Clock. When this pin is used UART1_RTS is not functional. Not available with the current firmware.
13	GPIO_12/UART1_CTS/I2S_WS/PCM_FSYNC	98	Input/Output	General Purpose Digital Input/Output Pin.
			Input	UART1_CTS – UART 1 Clear To Send. This pin is

S.No.	Pin Name	Pin number	Direction	Pin Description
				configured as UART pin based on host selection configuration. When this pin is used, I2S_WS/PCM_FSYNC is not functional.
			Input	I2S_WS – I2S Word Select. When this pin is used UART1_CTS is not functional. Not available with the current firmware.
			Input	PCM_FSYNC – PCM Frame Sync. When this pin is used UART1_CTS is not functional. Not available with the current firmware.
14	GPIO_13/I2S_DIN/PCM_MOSI/DBG_UART_RX	71	Input/Output	General Purpose Digital Input/Output Pin.
			Input	I2S_DIN – I2S interface input data. Not available with the current firmware.
			Input	PCM_MOSI – PCM interface Master-Out-Slave-In. Not available with the current firmware.
			Input	DBG_UART_RX – Debug UART receive pin.
15	GPIO_14/I2S_DOUT/PCM_MISO/DBG_UART_TX	9	Input/Output	General Purpose Digital Input/Output Pin.
			Output	I2S_DOUT – I2S interface output data. Not available with the current firmware.
			Output	PCM_MISO – PCM interface Master-In-Slave-Out. Not available with the current firmware.
			Output	DBG_UART_TX – Debug UART transmit pin.

S.No.	Pin Name	Pin number	Direction	Pin Description
16	GPIO_15/BT_LDR_BPS/PS_WAKEUP	29	Input/Output	General Purpose Digital Input/Output Pin. Reserved
			Input	BT_LDR_BPS – Boot loader bypass pin is used during powering up, high on this pin will bypass the boot loader.
			Input	PS_WAKEUP – Power save wake up pin is used in power save modes to wake up the module. High on this pin will wake up the module from power save mode.
17	GPIO_16/LED0	28	Input/Output	General Purpose Digital Input/Output Pin. Reserved
			Output	LED0 – Control signal for external LED 0. This function is used for future use.
18	GPIO_17/WLAN_ACTIVE	84	Input/Output	GPIO_17 – Reserved
			Output	WLAN_ACTIVE – Used for External BT, It Indicates with Logic high that wlan activity is in progress. When Low, BT device has the opportunity to transmit. If external BT.not used should be left NC.
19	GPIO_18/BT_PRIORITY	82	Input/Output	Reserved Default
			Input	BT_PRIORITY - Used to indicate through logic high that BT is transmitting high priority traffic. If external BT not used should be pulled down through 100K ohm Resistor.
20	GPIO_19/BT_ACTIVE	21	Input/Output	Reserved Default
			Input	This pin is asserted by an external BT device indicating that it wants to send data.
21	GPIO_21/PS_SL	81	Input/Output	GPIO_21 –Reserved

S.No.	Pin Name	Pin number	Direction	Pin Description
	P		Output	PS_SLP – Power save sleep is used in power save modes, High indicates device is out of sleep. If not used should be left NC.

Table 8: GPIO Interface

Note: GPIO_1,3,4,5,6 have a pull up resistor of 100K, These pull ups are used in reducing the current consumption in ULP deep sleep Mode.

4.1.2.5 JTAG Interface

All JTAG signals of type LVCMOS are rated at 4mA.

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	JP0	69	Input	Reserved (connect to ground through 1k ohms resistor).
2.	JP2	96	Input	Reserved (connect to ground through 1k ohms resistor).
3.	JNC	97	Output	Reserved (leave this pin as NC).
4.	JP1	70	Input	Reserved (connect to ground through 1k ohms resistor).

Table 9: JTAG Interface

4.1.2.6 Analog Interface

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	AUX_DAC_OUT	93	Output	Reserved.
2.	AUX_ADC_IN0	65	Input	Leave this pin as NC.

Table 10: Analog Interface

4.1.2.7 PMU Interface

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	VOUTLDOP1	92	Output	USB mode: This pin should be connected to USB_VDDD pin (pin # 15).
			Input/Output	Other modes: Leave this pin as NC.
2.	VOUTLDOP3	66	Output	USB mode: This pin should be to USB_VDDP pin (pin # 77).
			Input/Output	Other modes: Leave this pin as NC.
3.	VOUTLDOP1A	63	Output	This pin should be connected to BBP_LMAC_VDD_12 (pin # 91).

Table 11: PMU Interface

4.1.2.8 ULP PMU Interface

All ULP PMU interface signals of type LVCMOS are rated at 4mA.

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	ULP_GPIO_0	3	Input/Output	Reserved. Should be pulled down through 100K ohm Resistor.
2.	ULP_GPIO_1	68	Input/Output	Reserved. Should be pulled down through 100K ohm Resistor.
3.	ULP_GPIO_2	99	Input/Output	Reserved. Should be pulled down through 100K ohm Resistor.
4.	ULP_ANAGPI	73	Input	Reserved.
5.	HOST_BB_EN	94	Output	Reserved.
6.	VBATT	100	Input	3.3V power supply

Table 12: ULP PMU Interface

4.1.2.9 Reset Latch Configuration

Some of the pins are used to configure the chip during the assertion duration of RESET_N by connecting or not connecting an external pull-down resistor (4.7 KΩ). The table below gives these details. In the Description column of the table below, 0 indicates that an external pull-down resistor is connected and 1 indicates that no external pull-down resistor is connected. Some of the pins are used to configure the chip under reset by adding a pull-up or pull-down. The table below gives these details.

S.No.	Pin Name	Pin number	Direction	Description
1.	BOOTLOAD_EN	41	Input	**Reserved.** At power-on this pin is configured as input. Default value: 1 Firmware version 1.0.1d and less than that should have a 4.7K ohm pull down resistor.
2.	BOOT_MODE_0	40	Input	In case of USB enumeration please add a 4.7k ohm pull down. In case of USB_CDC this pin should be NC.
3.	HOST_SEL_0	60	Input	At power-on these pins are configured as input. Default value: 11 {HOST_SEL_1,HOST_SEL_0} 00: Reserved 01: To select USB host interface 10: To select SPI host interface 11: To select SDIO host interface Refer MIG for further details.
4.	HOST_SEL_1	55	Input	

Table 13: Reset Latch Configuration

Notes: Some interfaces are not used in the default configuration or mode of operation. These include the I2C, I2S, PCM, SSI, GSPI, LED, GPIO and UART interfaces. These may be used in custom applications with appropriate firmware. These are all fundamentally Input/Output signals and may be configured either as input or output.

- Please refer to the Module Integration Guide document for reference schematics.
- Please contact Redpine Signals, Inc for application notes or for customization of a solution.

4.2 Pin Description for module with integrated antenna

4.2.1 Module pinout diagram

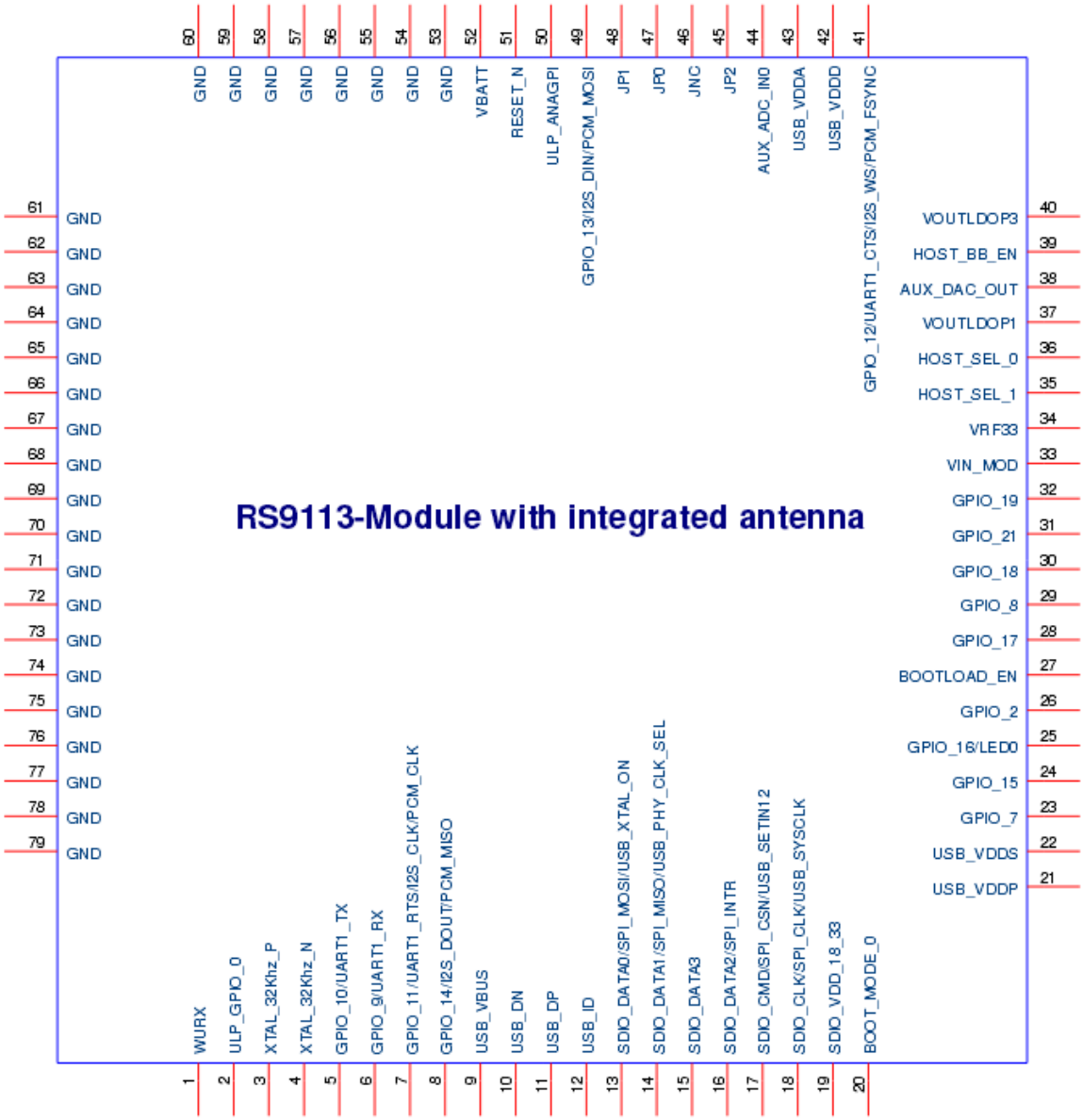


Figure 9: Module Pinout Diagram

4.2.2 Pin Description

4.2.2.1 Power and Ground Interface

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	SDIO_VDD_18_	19	Input	SDIO mode: 1.8V or 3.3V

S.No.	Pin Name	Pin number	Direction	Pin Description
	33			digital power supply. Based on SDIO data lines operating voltage.
			Input	Other modes: 3.3V digital power supply.
2.	USB_VDDA	43	Input	USB mode: 3.3V analog power supply.
			Input	Other modes: Connect this pin to ground.
3.	USB_VDDS	22	Input	USB mode: 3.3V digital power supply.
			Input	Other modes: Connect this pin to ground.
4.	USB_VDDP	21	Input	USB mode: 1.2V analog power supply. This pin should be connected to VOUTLDOP3 pin (pin # 40). No external supply needed
			Input	Other modes: Connect this pin to ground.
5.	USB_VDDD	42	Input	USB mode: 1.2V digital power supply. This pin should be connected to VOUTLDOP1 pin (pin # 37). No external supply needed
			Input	Other modes: Connect this pin to ground.
6.	VIN_MOD	33	Input	3.3V analog power supply for power management section of RS9113 module.
7.	VRF33	34	Input	3.3V analog power supply for RF transceiver. Refer MIG for power supply filter.
8.	GND	53,54,55,56, 57,58,59,60, 61,62,63,64, 65,66,67,68, 69,70,1,72,	Ground	Common ground

S.No.	Pin Name	Pin number	Direction	Pin Description
		73,74,75,76, 77,78,79		

Table 14: Power and Ground Interface

4.2.2.2 Control Interface

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	XTAL_32Khz_N	4	Input	32kHz off-chip crystal connections to ULP PMU for accurate wake-up time. Not supported in the current firmware. should be left open.
2.	XTAL_32Khz_P	3	Input	
3.	RESET_N	51	Input	Active-low asynchronous reset signal. The reset assertion time is about 20ms.
4.	WURX	1	Input	This pin is used for wireless RF wake-up. If RF wake-up feature is used, then route the PCB trace from the output of this pin, as a 50 ohms RF line. Not supported in the current firmware. should be left open..

Table 15: Control Interface

4.2.2.3 SDIO and USB Interface

The following table lists the pins used to connect to an MCU with the RS9113 being a slave, using SDIO, or USB. The pins are configured for a particular interface by controlling the HOST_SEL[1:0] reset latches- please refer to section 4.2.2.9 for further details on reset latch configuration. All SDIO signals of type LVCMOS are rated at 8mA. All USB signals except USB_VBUS are analog signals. USB_VBUS is a 5V pin.

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	SDIO_CLK/SPI_CLK/USB_SYSCLK	18	Input	SDIO Mode: This signal is SDIO clock.
			Input	SPI mode: This signal is SPI clock.
			Input	USB Mode: Reserved.
2.	SDIO_CMD/SPI_CSN/USB_SETIN12	17	Input/Output	SDIO Mode: SDIO interface command signal.
			Input	SPI Mode: Active-low SPI Chip-Select signal.
			Input	USB Mode: Reserved.
3.	SDIO_DATA0/SPI_MOSI/USB_XTAL_ON	13	Input/Output	SDIO Mode: Data0 of SDIO interface.
			Input	SPI Mode: SPI Master-Out-Slave-In.
			Output	USB Mode: Reserved.
4.	SDIO_DATA1/SPI_MISO/USB_PHY_CLK_SEL	14	Input/Output	SDIO Mode: Data1 of SDIO interface.
			Output	SPI Mode: SPI Master-In-Slave-Out.
			Input	USB Mode: Connect this pin to ground through a 4.7k ohms pull-down resistor.

S.No.	Pin Name	Pin number	Direction	Pin Description
5.	SDIO_DATA2/SPI_INTR	16	Input/Output	SDIO Mode: Data2 of SDIO interface.
			Output	SPI Mode: Interrupt signal to Host MCU. Active-high level, Active-low level and open-drain modes are supported.
			Input/Output	USB Mode: Reserved.
6.	SDIO_DATA3	15	Input/Output	SDIO Mode: Data3 of SDIO interface.
			Output	SPI Mode: Active-high level interrupt to Host indicating an error on the SPI bus. When this signal goes high, it indicates that the internal processor has reset the SPI interface due to an error reported by the interface. The Host MCU has to suspend all SPI transactions and re-initialize the SPI once this signal goes low.
			Input/Output	USB Mode: Leave this pin as NC.
7.	USB_VBUS	9	Input	USB mode: 5V power supply.
			Input/Output	Other modes: Leave this pin as NC.
8.	USB_DN	10	Input/Output	USB mode: Negative output channel that is connected to the serial USB cable.
			Input/Output	Other modes: Leave this pin as NC,
9.	USB_DP	11	Input/Output	USB mode: Positive output channel that is connected to the serial USB cable.

S.No.	Pin Name	Pin number	Direction	Pin Description
			Input/Output	Other modes: Leave this pin as NC.
10.	USB_ID	12	Input/Output	USB mode: Connect the USB ID pin to mini-AB receptacle connector.
			Input/Output	Other modes: Leave this pin as NC.

Table 16: SDIO Slave-SPI and USB interface

4.2.2.4 GPIO Interface

The RS9113 module has General Purpose I/Os, each with multiple alternate functionalities. All the GPIO pins are reserved by default with exception for few pins described below in the table. Custom firmware modifications are required to enable them to be used as GPIO input/output pins with exception for UART (TX, RX, RTS and CTS) interface. On power up all the GPIO's are Input until the firmware inside the module takes over the default input state.

All GPIO signals of type LVCMOS are rated at 4mA.

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	GPIO_2	26	Input/Output	This pin is configured as Output pin in power save modes. If not used leave this pin as NC.
2.	GPIO_7	23	Input/Output	Reserved.
3.	GPIO_8	29	Input/Output	Reserved.
4.	GPIO_9/UART1_RX	6	Input/Output	General Purpose Digital Input/Output Pin
			Input	UART1_RX – UART 1 Serial Input. This pin is configured as UART pin based on host selection configuration.
5.	GPIO_10/UART1_TX	5	Input/Output	General Purpose Digital Input/Output Pin
			Output	UART1_TX – UART 1 Serial Output. This pin is configured

S.No.	Pin Name	Pin number	Direction	Pin Description
				as UART pin based on host selection configuration.
6.	GPIO_11/UART1_RTS/I2S_CLK/PCM_CLK	7	Input/Output	General Purpose Digital Input/Output Pin
			Output	UART1_RTS – UART 1 Request To Send. This pin is configured as UART pin based on host selection configuration. When this pin is used, I2S_CLK/PCM_CLK is not functional.
			Input	I2S_CLK – I2S Clock. When this pin is used, UART1_RTS is not functional. Not available with the current firmware.
			Input	PCM_CLK – PCM Clock. When this pin is used, UART1_RTS is not functional. Not available with the current firmware.
7.	GPIO_12/UART1_CTS/I2S_WS/PCM_FSYNC	41	Input/Output	General Purpose Digital Input/Output Pin
			Input	UART1_CTS – UART 1 Clear To Send. This pin is configured as UART pin based on host selection configuration. When this pin is used, I2S_WS/PCM_FSYNC is not functional.
			Input	I2S_WS – I2S Word Select. When this pin is used, UART1_CTS is not functional. Not available with the current firmware.
			Input	PCM_FSYNC – PCM Frame Sync. When this pin is used, UART1_CTS is not functional. Not available with the current firmware.
8.	GPIO_13/I2S_DIN/PCM_MOSI/D	49	Input/Output	General Purpose Digital Input/Output Pin.

S.No.	Pin Name	Pin number	Direction	Pin Description
	BG_UART_RX		Input	I2S_DIN – I2S interface input data. Not available with the current firmware.
			Input	PCM_MOSI – PCM interface Master-Out-Slave-In. Not available with the current firmware.
			Input	DBG_UART_RX – Debug UART receive pin.
9.	GPIO_14/I2S_DOUT/PCM_MISO/DBG_UART_TX	8	Input/Output	General Purpose Digital Input/Output Pin.
			Output	I2S_DOUT – I2S interface output data. Not available with the current firmware.
			Output	PCM_MISO – PCM interface Master-In-Slave-Out. Not available with the current firmware.
			Output	DBG_UART_TX – Debug UART transmit pin.
10	GPIO_15/BT_LDR_BPS/PS_WAKEUP	24	Input/Output	General Purpose Digital Input/Output Pin.Reserved.
			Input	BT_LDR_BPS – Boot loader bypass pin is used during powering up, high on this pin will bypass the boot loader.
			Input	PS_WAKEUP – Power save wake up pin is used in power save modes to wake up the module. High on this pin will wake up the module from power save mode.
11	GPIO_16/LED0	25	Input/Output	General Purpose Digital Input/Output Pin
			Output	LED0 – Control signal for external LED 0. This function is used for future use.
12	GPIO_17/WLAN_	28	Input/Output	GPIO_17 – Reserved

S.No.	Pin Name	Pin number	Direction	Pin Description
	ACTIVE		Output	WLAN_ACTIVE – Used for External BT, It Indicates with Logic high that wlan activity is in progress. When Low, BT device has the opportunity to transmit. If not used should be left NC.
13	GPIO_18/BT_PRIORITY	30	Input/Output	Reserved
			Input	BT_PRIORITY - Used to indicate through logic high that BT is transmitting high priority traffic. If not used should be pulled down through 100K ohm Resistor.
14	GPIO_19/BT_ACTIVE	32	Input/Output	Reserved
			Input	This pin is asserted by an external BT device indicating that it wants to send data.
15	GPIO_21/PS_SLP	31	Input/Output	Reserved
			Output	PS_SLP – Power save sleep is used in power save modes, High indicates device is out of sleep. If not used should be left NC.

Table 17: GPIO Interface

4.2.2.5 JTAG interface

All JTAG signals of type LVCMOS are rated at 4mA.

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	JP0	47	Input	Reserved (connect to ground through 1k ohms resistor).
2.	JNC	46	Output	Reserved (leave this pin as NC).

S.No.	Pin Name	Pin number	Direction	Pin Description
3.	JP1	48	Input	Reserved (connect to ground through 1k ohms resistor).
4.	JP2	45	Input	Reserved (connect to ground through 1k ohms resistor).

Table 18: JTAG Interface

4.2.2.6 Analog Interface

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	AUX_DAC_OUT	38	Output	Reserved.
2.	AUX_ADC_IN0	44	Input	Leave this pin as NC.

Table 19: Analog Interface

4.2.2.7 PMU Interface

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	VOUTLDOP1	37	Output	USB mode: This pin should be connected to USB_VDDD pin (pin # 42).
			Input/Output	Other modes: Leave this pin as NC.
2.	VOUTLDOP3	40	Output	USB mode: This should be connected to USB_VDDP pin (pin # 21).
			Input/Output	Other modes: Leave this pin as NC.

Table 20: PMU Interface

4.2.2.8 ULP PMU interface

All ULP PMU interface signals of type LVCMOS are rated at 4 mA.

S.No.	Pin Name	Pin number	Direction	Pin Description
1.	ULP_GPIO_0	2	Input/Output	Reserved. Should be pulled down through 100K ohm Resistor.
2.	ULP_ANAGPI	50	Input	Reserved.
3.	HOST_BB_EN	39	Output	Reserved.
4.	VBATT	52	Input	3.3V input power supply.

Table 21: ULP PMU interface

4.2.2.9 Reset Latch Configuration

Some of the pins are used to configure the chip during the assertion duration of RESET_N by connecting or not connecting an external pull-down resistor (4.7 KΩ). The table below gives these details. In the Pin Description column of the table below, 0 indicates that an external pull-down resistor is connected and 1 indicates that no external pull-down resistor is connected. Some of the pins are used to configure the chip under reset by adding a pull-up or pull-down. The table below gives these details.

S.No.	Pin Name	Pin number	Direction	Description
1.	BOOTLOAD_EN	27	Input	At power-on this pin is configured as input. Default value: 1 Firmware version 1.0.1d and less than that should have a 4.7K ohm pull down resistor.
2.	BOOT_MODE_0	20	Input	In case of USB enumeration please add a 4.7k ohm pull down. In case of USB_CDC this pin should be NC.
3.	HOST_SEL_0	36	Input	At power-on these pins

S.No.	Pin Name	Pin number	Direction	Description
4.	HOST_SEL_1	35	Input	are configured as input. Default value: 11 {HOST_SEL_1,HOST_SEL_0} 00: Reserved. 01: To select USB host interface. 10: To select SPI host interface. 11: To select SDIO host interface. Refer MIG for further details.

Table 22: Reset latch configuration

Notes:

Some interfaces are not used in the default configuration or mode of operation. These include the I2C, I2S, PCM, SSI, GSPI, Analog, LED, GPIO, and UART interfaces. These may be used in custom applications with appropriate firmware. These are all fundamentally Input/Output signals and may be configured either as input or output.

- Please refer to the Module Integration Guide document for reference schematics.
- Please contact Redpine Signals, Inc for application notes or for customization of a solution.

5 Functional overview

5.1 Clocks

- By default software programs the clock source to 40 MHz.
- If required, software can configure the clock to higher frequency up to a maximum of 118 MHz.
- A hardware clock manager controls clocks to different modules in RS9113 module.
- Clock manager switches to host clock during sleep mode.

5.1.1 Sleep Mode Clock

The device by default runs on an internal RC oscillator. For better accuracy, the device can be connected to an external 32.768 KHZ (MC146) crystal as per the guidelines in the Module Integration Guide (MIG) guide.

5.2 Boot Modes

- At start up, boot pins are used to select boot options.
- The boot loader is located in ROM.
- Boot mode can be configured through Reset latches as described in "Reset latch configuration" section.

5.3 Host Interface Selection

The RS9113 module supports the following host interfaces. Only one of or SDIO or USB interface can be active at any given time.

HOST_SEL_1	HOST_SEL_0	Interface
High	High	SDIO(default)
Low	High	USB

Table 23: Host interface selection

5.4 General-purpose input/outputs (GPIOs)

- Each pin can be programmed as an output or as an input port for various functions.
- All GPIO pins are configured as inputs on power-up, and they remain as inputs until configured otherwise. All unused GPIO pins are configured as outputs. GPIO pins may have alternate input and output functions supporting UART, LED, I2S, SPI, Debug UART and PCM. These alternate functions can be selected using GPIO mode selection

5.5 Inter-integrated Sound Interface (I2S)

- The module supports only slave mode
- Philips Inter-IC sound Bus specifications compliant
- Support for one stereo channel in transmitter and one stereo channel in receiver
- Supports 12 and 16 bit resolutions as an input or output channel.
- It uses an external clock source.
- Audio sampling frequencies from 8 KHz up to 44.1 KHz are supported.
- Maximum operating frequency is 33 MHz.

5.6 PCM Interface

- The PCM interface of RS9113 module works in slave mode which can transmit and receive serial data to and from an off-chip PCM master.
- Supports full-duplex data transfer with a PCM master.
- Supports 8, 12, 16, 24 and 32-bit frame sizes.
- Data is driven at the rising edge of clock and sampled at the falling edge of clock.
- Maximum operating frequency is 33 MHz.

5.7 UART Interface

- The module supports one UART interface.
- Supports 5,6,7 and 8 bit encoding
- Supports 1,1.5 and 2 stop bits
- Supports Auto flow control.
- Supports even, odd and no parity.
- Supports standard baud rates of 9600,19200,38400,57600,115200,230400,460800,921600 bits per second (bps).

5.8 LED Interface

- Control signals can be generated over this interface to control external LEDs.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Absolute maximum ratings in the table given below are the values beyond which the device could be damaged. Functional operation at these conditions or beyond these conditions is not guaranteed.

Parameter	Symbol	Value	Units
Input supply voltage	VIN_MOD, SDIO_VDD_18_33	3.6	V
USB VBUS voltage	USB_VBUS	5.2	V
Input supply voltage for SDIO interface	SDIO_VDD_18_33	3.6	V
Input analog voltage for USB	USB_VDDA	3.6	V
Input digital voltage for USB	USB_VDDS	3.6	V
Input supply voltage	VBATT	3.6	V
Input analog supply voltage for RF	VRF33	3.6	V
Input digital supply voltage for RF	VDD33	3.6	V
RF Input Level	RF_OUT_1, RF_OUT_2	10	dBm
Storage temperature	T_{store}	-65 to 150	°C
Operating temperature range	T_{op}	-40 to 85	°C
Electrostatic discharge tolerance (HBM)	ESD_{HBM}	2000	V
Electrostatic discharge tolerance (MM)	ESD_{MM}	200	V
Electrostatic discharge tolerance (CDM)	ESD_{CDM}	500	V

Table 24: Absolute maximum ratings

6.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Input supply voltage	SDIO_VD	3.0	3.3	3.6	V

	D_18_33				
Input supply voltage	VIN_MOD	3.0	3.3	3.6	V
Input supply voltage	VBATT	3.0	3.3	3.6	V
Input supply voltage for SDIO Interface	SDIO_VDD_18_33	1.8	3.3	3.6	V
Input digital supply voltage for USB interface	USB_VDDS	3.0	3.3	3.6	V
Input analog supply voltage for USB analog portions	USB_VDDA	3.0	3.3	3.6	V
Input analog supply Voltage for RF	VRF33	3.0	3.3	3.6	V
Input digital supply voltage for RF	VDD33	3.0	3.3	3.6	V
Ambient temperature	T_a	-40	25	+85	°C

Table 25: Recommended Operating Conditions

6.3 DC Characteristics – Digital I/O Signals

Parameter	Min.	Typ.	Max.	Units
Input high voltage	2	-	3.6	V
Input low voltage	-0.3	-	0.8	V
Output low voltage	-	-	0.4	V
Output high voltage	2.4	-	-	V
Input leakage current (at 3.3V or 0V)	-	-	±10	µA
Tristate output leakage current (at 3.3V or 0V)	-	-	±10	µA

Table 26: Input/Output DC characteristics

6.4 AC characteristics – digital I/O signals

6.4.1 SDIO Interface

6.4.1.1 Full Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SDIO_CLK Period	T_{sdio}	40	-	-	ns

Parameter	Symbol	Min.	Typ.	Max.	Units
sdio_data_in, setup time	T_s	5	-	-	ns
sdio_data_in, hold time	T_h	5	-	-	ns
sdio_data_out, clock-to-output valid, during data transfer	T_{odd}	0	-	14	ns
sdio_data_out, clock-to-output valid, during identification	T_{odi}	0	-	50	ns
Output Load		0		40	pF

Table 27: AC characteristics - SDIO full speed mode (protocol)

Parameter	Symbol	Min.	Typ.	Max.	Units
SDIO_CLK Period	T_{sdio}	40	-	-	ns
sdio_data_in, setup time	T_s	4	-	-	ns
sdio_data_in, hold time	T_h	1	-	-	ns
sdio_data_out, clock-to-output valid, during data transfer	T_{odd}	0	-	12	ns
sdio_data_out, clock-to-output valid, during identification	T_{odi}	0	-	50	ns
Output Load		0		40	pF

Table 28: AC characteristics - SDIO full speed mode (on silicon)

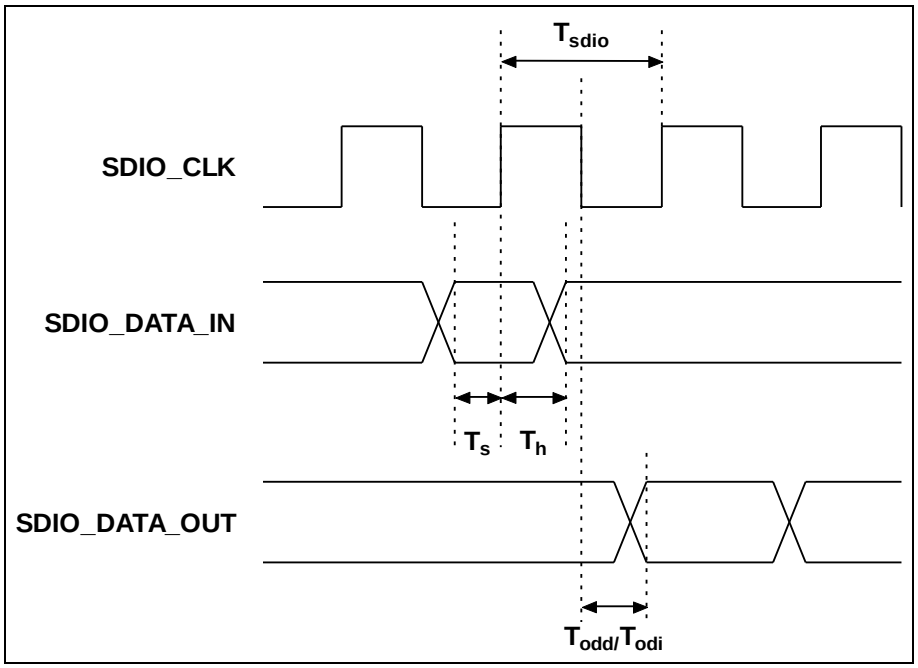


Figure 10: SDIO interface timings - full speed mode

6.4.1.2 High Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SDIO_CLK Period	T_{sdio}	20	-	-	ns
sdio_data_in, setup time	T_s	6	-	-	ns
sdio_data_in, hold time	T_h	2	-	-	ns
sdio_data_out, clock-to-output valid	T_{od}	-	-	14	ns
Output Load		0		40	pF

Table 29: AC characteristics - SDIO high speed mode (protocol)

Parameter	Symbol	Min.	Typ.	Max.	Units
SDIO_CLK Period	T_{sdio}	20	-	-	ns
sdio_data_in, setup time	T_s	4	-	-	ns
sdio_data_in, hold time	T_h	1	-	-	ns
sdio_data_out, clock-to-output valid	T_{od}	-	-	12	ns

Parameter	Symbol	Min.	Typ.	Max.	Units
Output Load		0		40	pF

Table 30: AC characteristics - SDIO high speed mode (on silicon)

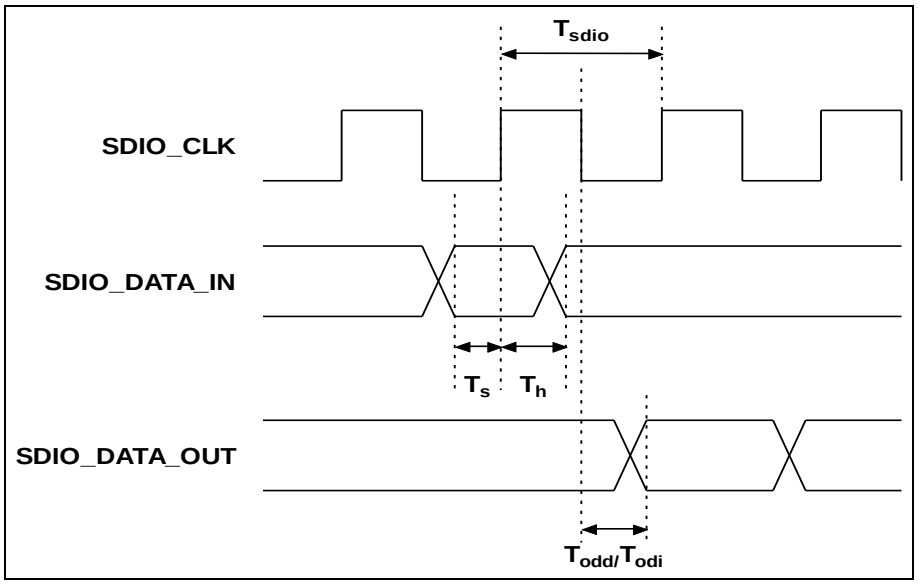


Figure 11: SDIO interface timings - high speed mode

6.4.2 Host SPI Interface

6.4.2.1 Low Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SPI_CLK Period	T_{spi}	40	-	-	ns
SPI_CS to output valid	T_{cs}	-	-	7.5	ns
SPI_CS, setup time	T_{cst}	5	-	-	ns
SPI_MOSI, setup time	T_{sd}	1.5	-	-	ns
SPI_MOSI, hold time	T_{hd}	1	-	-	ns
SPI_MISO, clock to output valid	T_{od}	-	-	10	ns
Output Load		0		10	pF

Table 31: AC characteristics - host SPI low speed mode

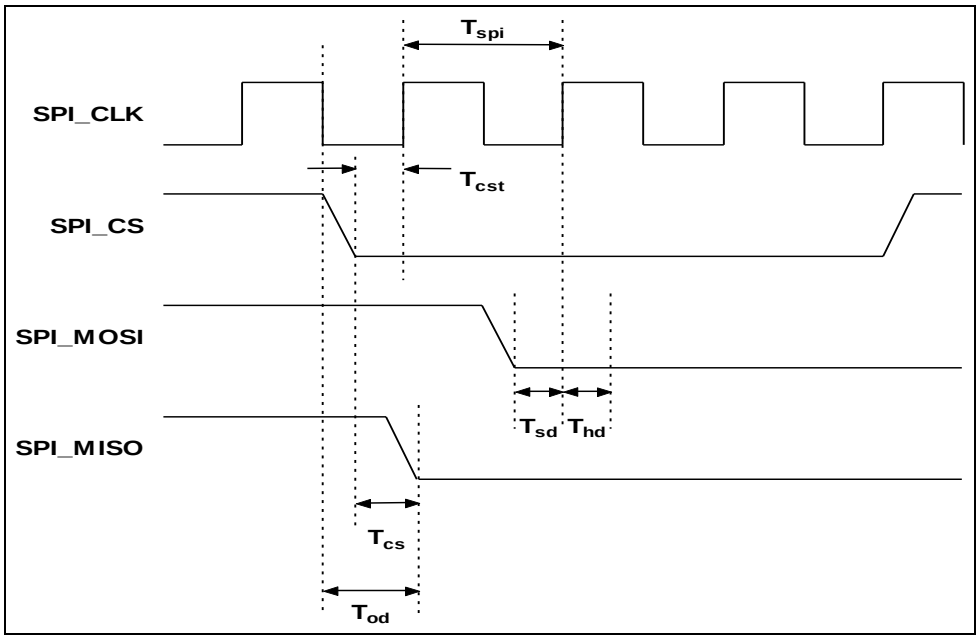


Figure 12: Interface timings - host SPI low speed mode

6.4.2.2 High Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SPI_CLK Period	T_{spi}	12.5	-	-	ns
SPI_CS to output valid	T_{cs}	-	-	7.5	ns
SPI_CS, setup time	T_{cst}	5	-	-	ns
SPI_MOSI, setup time	T_{sd}	1	-	-	ns
SPI_MOSI, hold time	T_{hd}	1	-	-	ns
SPI_MISO, clock to output valid	T_{od}	2.5	-	8.75	ns
Output Load		0		10	pF

Table 32: AC characteristics - host SPI high speed mode

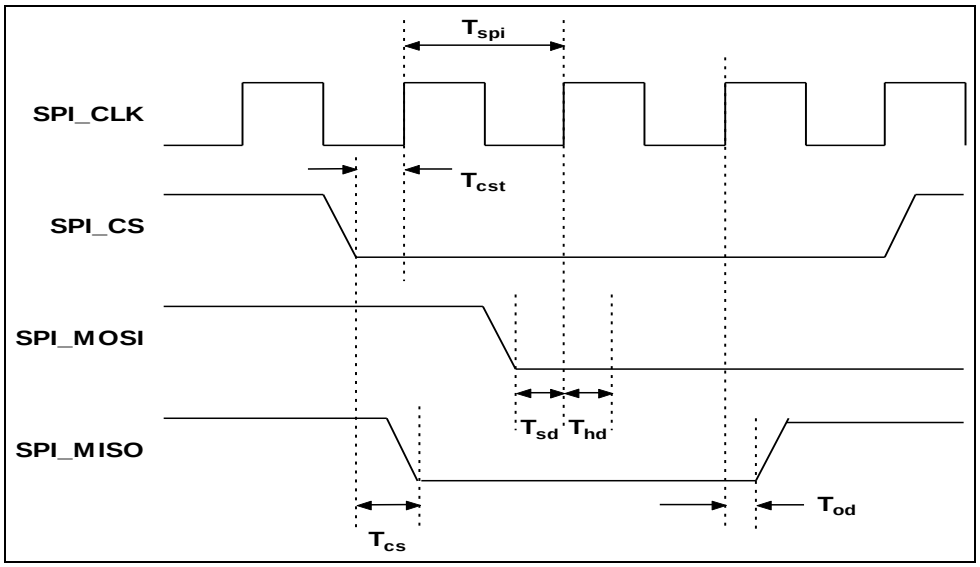


Figure 13: Interface timings – host SPI high speed mode

6.4.3 USB Interface

6.4.3.1 Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Trise	1.5Mbps 12Mbps 480Mbps	75 4 0.5	-	300 20	ns
Tfall	1.5Mbps 12Mbps 480Mbps	-	-	7.5	ns
Jitter	1.5Mbps 12Mbps 480Mbps	5	-	-	ns

Table 33: USB Interface - Timing Characteristics

6.4.3.2 Electrical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
V_{cm} DC (DC level measured at	HS Mode LS/FS Mode	-0.05 0.8	-	0.5 2.5	V

Parameter	Conditions	Min.	Typ.	Max.	Units
receiver connector)		0.5			
Crossover Voltages	LS Mode FS Mode	1.3 1.3	-	2 2	V
Power supply ripple noise (Analog 3.3V)	<160MHz	-50	0	50	mV
Power supply ripple noise (Analog 1.2V)	<2MHz	-10	0	10	mV
	>2MHz	-50	0	50	
Power supply ripple noise CORE(Digital 1.2V)	All conditions	-50	0	50	mV

Table 34: USB interface - electrical characteristics

6.4.4 I2S Interface

Parameter	Symbol	Min.	Typ.	Max.	Units
i2s_clk	Tclk	0	-	30	ns
i2s_din,i2s_ws setup time	Tsetup	5	-		ns
i2s_din,i2s_ws hold time	Thold	2	-	-	ns
i2s_dout output delay	Tdout	10	-	-	ns
i2s_dout output load	Tod	0		40	pF

Table 35: AC characteristics - I2S

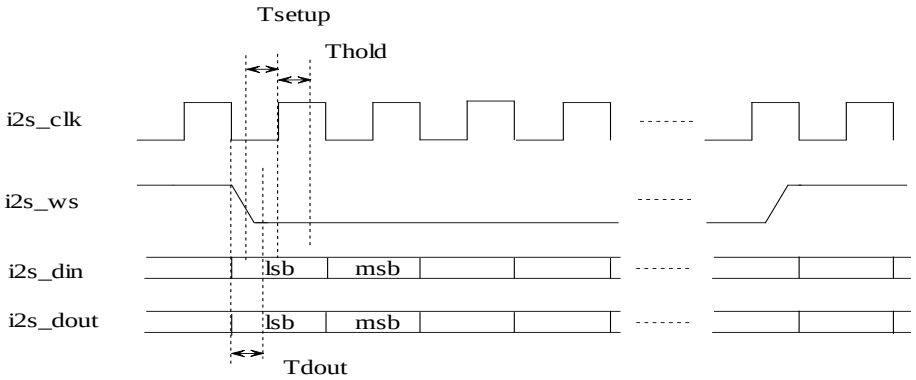


Figure 14: Interface timings - I2S

6.5 Reset timing

Following diagram shows the timing requirement for reset input in two scenarios.

A. Power up

B. Giving reset during module operation

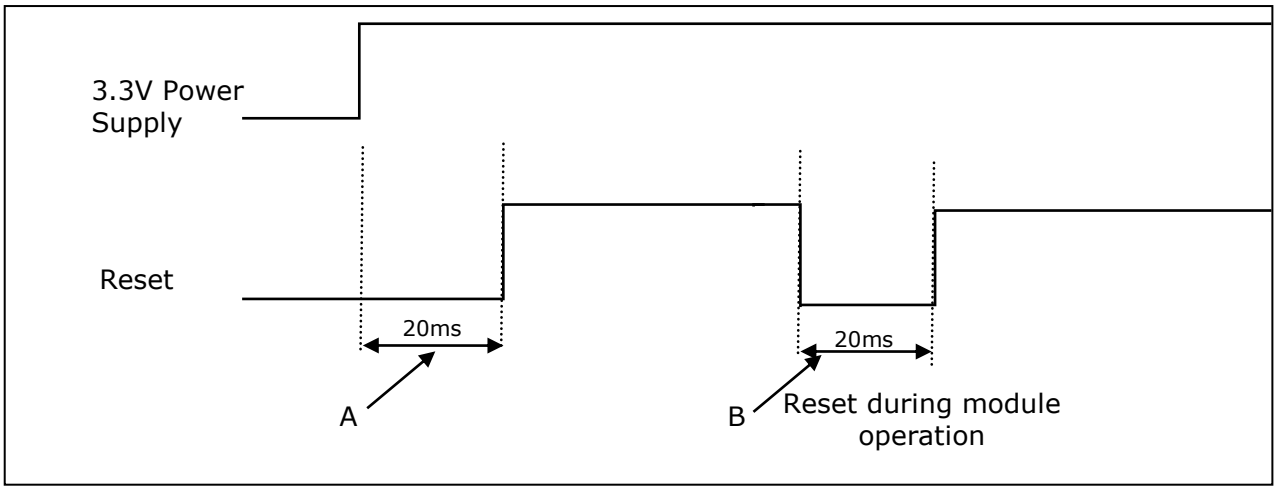


Figure 15: Reset timing diagram

7 Performance specifications

7.1 Wi-Fi specifications

Feature	Description
Network Standard Support	IEEE 802.11a/b/g, 802.11n, 802.11d/e/i/, , 802.11/r/, 802.11h
Frequency Band	2.400 – 2.500 GHz 4.900 – 5.850 GHz
Modulation	OFDM with BPSK, QPSK, 16-QAM, and 64-QAM 802.11b with CCK and DSSS
Supported Data Rates in Mbps	802.11n: MCS 0 –MCS7 (20/40Mhz), MCS32, Short GI. 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11b: 1, 2, 5.5, 11 Mbps
802.11n Advanced Features	1-SS, 40MHz bandwidth, greenfield preamble, short-GI, RIFS, A-MPDU, A-MSDU aggregation with block-ack, fragmentation and virtual AP support (up to 4 BSSIDs).
Wi-Fi Modes	Wi-Fi client, Access point, Wi-Fi Direct, Simultanious client and Access Point.
Typical WLAN Transmit Power (+/- 2 dBm)	18 dBm for 802.11b CCK 18 dBm for 802.11g/n OFDM 14 dBm for 802.11a/nOFDM

Table 36: Wi-Fi specifications

7.2 Bluetooth specifications

Feature	Description
Network Standard Support	Bluetooth v2.1 + EDR, , BLE v4.0
Frequency Band	2.402 GHz - 2.480 GHz
Modulation	GFSK, DQPSK, 8DPSK
Supported Data Rates	1, 2, 3 Mbps
Bluetooth Advanced Features	Adaptive frequency hopping, interlaced scanning, 7 active slaves Supports , hold, sniff and park modes
Bluetooth modes	Master, slave

Feature	Description
Typical BT Transmit Power(+/- 2dBm)	18 dBm for Bluetooth GFSK, DQPSK, 8DPSK

Table 37: Bluetooth specifications

7.3 ZigBee specifications

Feature	Description
Network Standard Support	ZigBee p802.15.4-2009 (2.4GHz)
Frequency Band	2.402 GHz - 2.480 GHz
Modulation	DSSS
Supported Data Rates	250 kbps
ZigBee Advanced Features	CCM security, orphan scanning, coordinator realignment, mesh routing
ZigBee modes	ZigBee Coordinator, Router, End device
Typical ZigBee Transmit Power	19 dBm

Table 38: ZigBee specifications

7.4 Receive characteristics

7.4.1 Wi-Fi receive sensitivity 40mHz

Data Rate	Typical Sensitivity (+/- 1.5 dB)
1 Mbps	-97.0 dBm (< 8% PER)
2 Mbps	-93.0 dBm (< 8% PER)
11 Mbps	-88.9 dBm (< 8% PER)
6 Mbps	-91.0 dBm (<10% PER)
54 Mbps	-74.5dBm (< 10% PER)
65 Mbps	-71.9 dBm (< 10% PER)

Table 39: Wi-Fi Receive Sensitivity 20Mhz

7.4.2 Bluetooth receive sensitivity

Data Rate	Typical Sensitivity (+/- 1.5 dB)
GFSK(1 Mbps)	-93 dBm
EDR-DQPSK(2 Mbps)	-92 dBm
EDR-D8PSK(3 Mbps)	-81.5 dBm

Data Rate	Typical Sensitivity (+/- 1.5 dB)
BT-LE(1 Mbps)	-93 dBm

Table 40: Bluetooth receive sensitivity

7.4.3 ZigBee receive sensitivity

Data Rate	Typical Sensitivity (+/- 1.5 dB)
250kbps	-103 dBm

Table 41: ZigBee receive sensitivity

8 Software architecture

The RS9113 modules is a host based architecture with OS providing the core functionality support for Wi-Fi, Bluetooth and ZigBee features. The kernel layer interfaces with host driver to provide functionality for different wireless modules.

The following block diagram illustrates the software architecture of OneBox™ mobile solution with WLAN, Bluetooth and ZigBee.

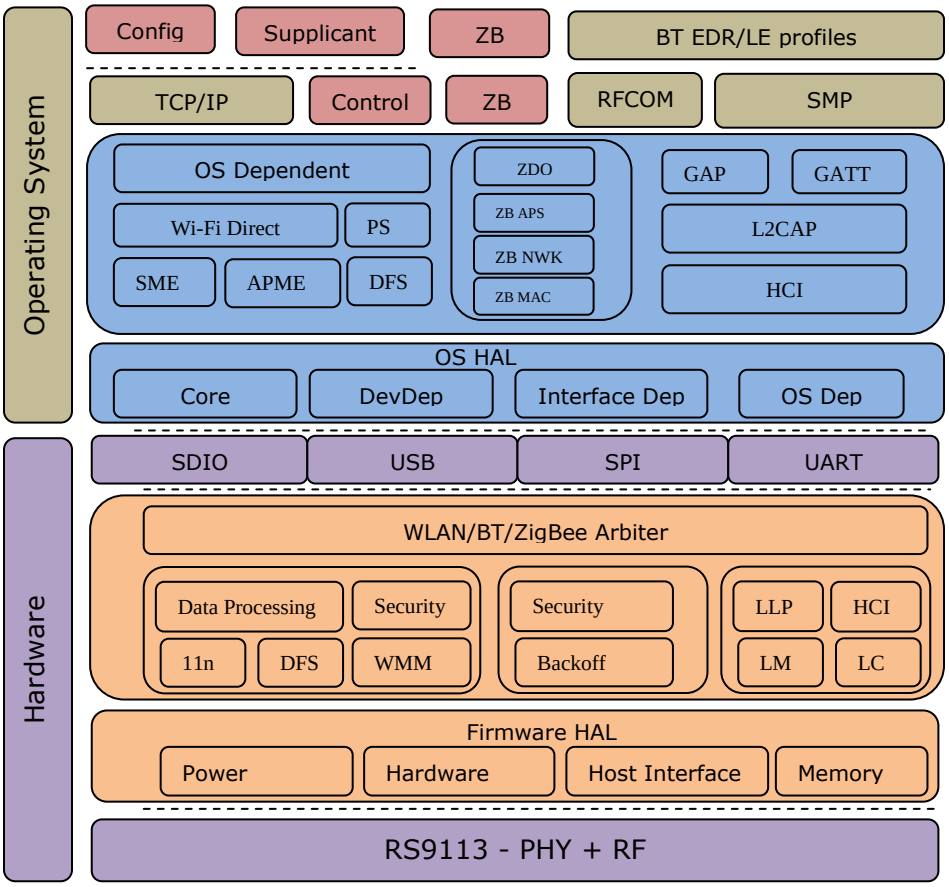
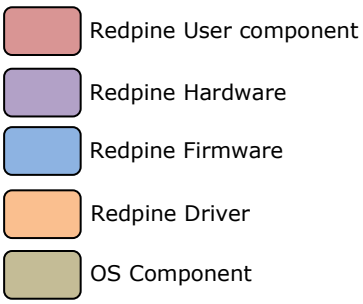


Figure 16: OneBox Mobile Software architecture diagram



8.1 Operating system support

The RS9113 module supports the following operating systems.

- Linux
- Android
- WinCE

9 Ordering information

9.1 Contact information

For additional information, please contact Sales at Redpine Signals, Inc.

Redpine Signals, Inc.

2107 North First Street, Suite 680,

San Jose, CA 95131 USA

Phone: +1 408 748 3385

E-mail: sales@redpinesignals.com

Website: http://www.redpinesignals.com/

9.2 Packing Tray Information

Each tray for package P7 can accommodate 70 modules please find the mechanical details of the tray below.

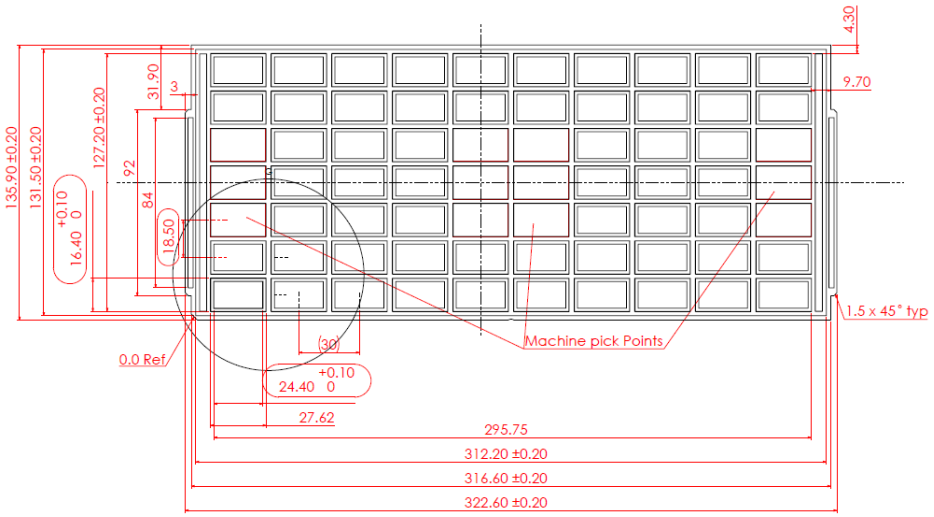


Figure 17 Tray Details For P7 Package

Each tray for package P6 can accommodate 84 modules please find the mechanical details of the tray below.

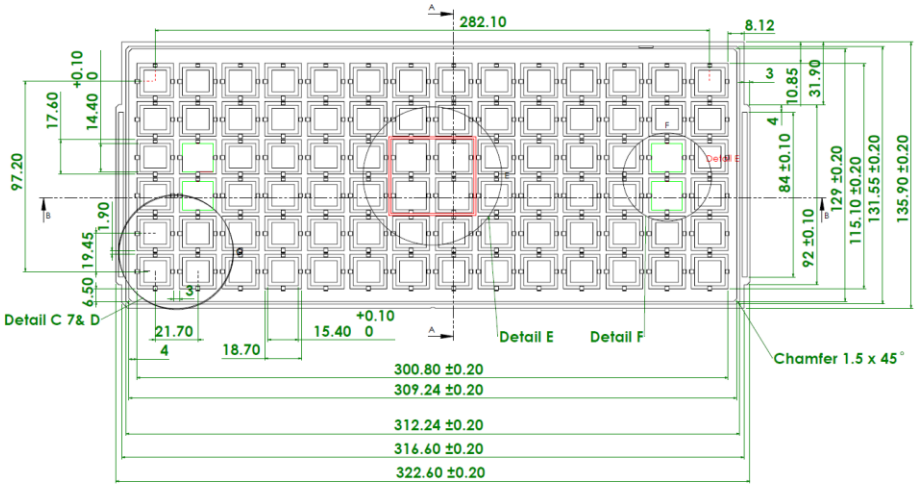
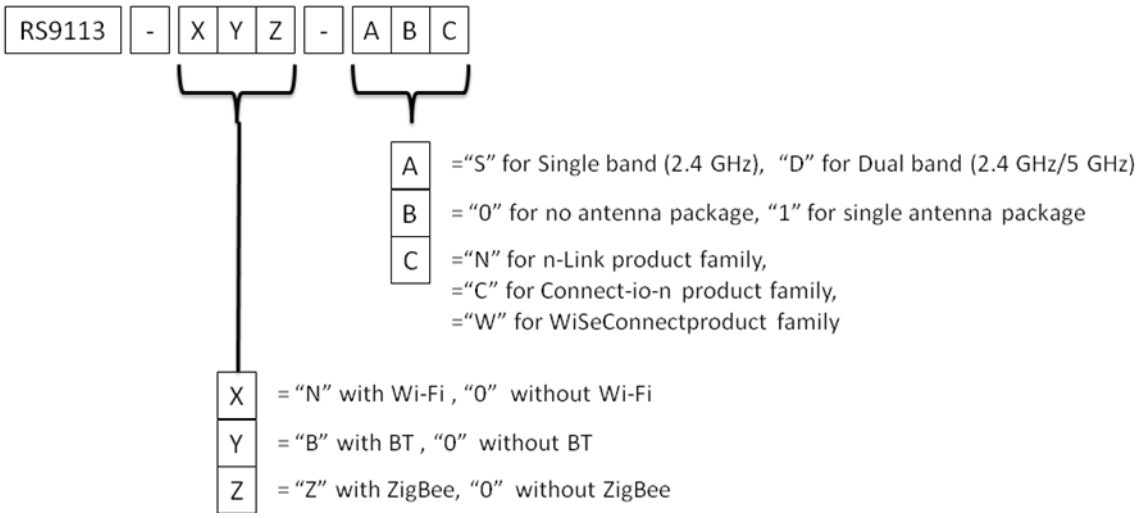


Figure 18

Tray Details For P6 Package

9.3 Device ordering information

The device numbering is based on the following naming convention. All the devices are labeled as RS9113-XYZ-ABC



Examples:

- RS9113-NBZ-S0N will refer to single band n-Link module with no antenna and integrated Wi-Fi, Bluetooth and ZigBee.
- RS9113-N00-D1C will refer to a dual band Connect-io-n module with embedded single antenna and integrated Wi-Fi.
- RS9113-NB0-S0W will refer to a single band WiSeConnect module with no antenna and integrated Wi-Fi and Bluetooth.

The naming for evaluation boards is similar to the naming convention as described above with a “–EVB” suffixed to the module part number such

as RS9113-XYZ-ABC-EVB.For example, RS9113-NBZ-S0N-EVB will refer to the evaluation board consisting of the RS9113-NBZ-S0N based module.

The following table lists the device part numbers to be used for ordering modules or evaluation boards. Redpine can create and provide customized firmware based on user requirements.

Device Number	Description	Packaging	Qualification
RS9113-N00-S0N	Single band n-Link module with no antenna and integrated Wi-Fi.	Tray	Industrial
RS9113-N00-D0N	Dual band n-Link module with no antenna and integrated Wi-Fi.	Tray	Industrial
RS9113-N00-S1N	Single band n-Link module with embedded single antenna and integrated Wi-Fi.	Tray	Industrial
RS9113-N00-D1N	Dual band n-Link module with embedded single antenna and integrated Wi-Fi.	Tray	Industrial
RS9113-NB0-S0N	Single band n-Link module with no antenna and integrated Wi-Fi and Bluetooth	Tray	Industrial
RS9113-NB0-D0N	Dual band n-Link module with no antenna and integrated Wi-Fi and Bluetooth	Tray	Industrial
RS9113-NB0-S1N	Single band n-Link module with embedded single antenna and integrated Wi-Fi and Bluetooth	Tray	Industrial
RS9113-NB0-D1N	Dual band n-Link module with embedded single antenna and integrated Wi-Fi and Bluetooth	Tray	Industrial
RS9113-N0Z-S0N	Single band n-Link module with no antenna and integrated Wi-Fi and ZigBee.	Tray	Industrial
RS9113-N0Z-D0N	Dual band n-Link module with no antenna and integrated Wi-Fi and ZigBee.	Tray	Industrial
RS9113-N0Z-S1N	Single band n-Link module with embedded single antenna and integrated Wi-Fi and ZigBee	Tray	Industrial
RS9113-N0Z-D1N	Dual band n-Link module with embedded single antenna and integrated Wi-Fi and ZigBee	Tray	Industrial
RS9113-NBZ-S0N	Single band n-Link module with no antenna and integrated Wi-Fi ,Bluetooth and ZigBee	Tray	Industrial
RS9113-NBZ-D0N	Dual band n-Link module with no antenna and integrated Wi-Fi, Bluetooth and ZigBee.	Tray	Industrial
RS9113-NBZ-S1N	Single band n-Link module with embedded single antenna and integrated	Tray	Industrial

	Wi-Fi, Bluetooth and ZigBee.		
RS9113-NBZ-D1N	Dual band n-Link module with embedded single antenna and integrated Wi-Fi, Bluetooth and ZigBee.	Tray	Industrial

Table 42: Device Ordering Information

9.4 Collateral

The following documentation and software are available along with the RS9113 n-Link module family.

- Evaluation Board with supported host interface
- Device drivers for Linux and Android.
- EVB user guide
- Software installation guide
- Driver configuration guide
- Module integration guide.

Revision history

Rev.	Ver. No.	Date	Changes
1.	1.0	September 2013	Preliminary version
2.	1.0	November 2013	Minor edits
3.	1.1	November 2013	1) Modified selective pins(GPIOs and others) to "Reserved" 2) Deleted BT coexistence section as WLAN ACTIVE and BT PRIORITY pins are not mentioned in the pinout diagram. 3) Modified power-save description. 4) Minor edits across sections
4.	1.2	February 2014	1) Added PCB landing pattern dimensions for Package # P6 and P7. 2) Edited top view picture of Package # P7.
5.	1.3	February 2014	1) Appended UART host interface in section 2.2.Edited section 2.7 (removed I2C) 2) Modified description for TEST_MODE,WURX pins in section 4.1.2.1 and WURX in 4.2.2.2 3) Updated sections 4.1.2.3 and 4.2.2.3 4) Updated pin description in sections 4.1.2.5 and 4.2.2.5 5) Updated section description and pin description at 4.1.2.9 and 4.2.2.9 6)Updated pin description for in section 4.1.2.7 and 4.1.2.8 7) Updated pin description (ULP_GPIO_0) in section 4.2.2.8. 8) Removed I2C and GSPI timing diagrams in section 5. 9) Removed I2C and GSPI timing diagrams in section 6.

6.	2.0	February 2014	1) Modified module pinout diagrams and edited pin descriptions. 2) Modified module and pcb landing pattern dimensions. 3) Removed bottom view pictures of modules. 4) Removed sections 5.5(GSPI), 5.6(I2C), 5.10(SSI). 5) Removed timing diagrams for GSPI and I2C in section 6.
7.	2.1	February 2014	1) Edited pin description for USB related pins, VBATT and SPI mode pins. 2) Edited electrical characteristics table with more power supply pins appended. 3) Removed top view pictures of the module. 4) Re-arranged table for mechanical characteristics to a different sub-section for both variants of the module. 5) Edited SDIO_CLK pin description 6) Section 3.3 - Added belt speed and number of reflows.
8.	2.2	March 2014	1) Table 8: Inserted pin description for GPIO_0 and GPIO_1 pins. 2) Section 4.2.2.4: Minor edit to section description. 4) Table 24: Inserted absolute maximum rating for USB_VBUS. 5) Table5: Added pin # 31 to NC
9.	2.3	May 2014	1) Edited pin description for ULP_ANAGPI in Table 12.
10.	2.4	September	1) Added packaging tray diagram 2) Power save pins description added on GPIO_2, GPIO_15, GPIO 21. 3) Added Edits on the Pin description tables 4) Landing patterns updated for both the modules.

			5) Description for BT Priority, Wifi Activity and BT Active added 7) Updated the Low power numbers.